

Abstract

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A Fast Power Efficient Equalization-Based Digital Background Calibration Technique for Pipelined ADC

A signed variable step size least mean squares (SVSS-LMS) technique is used to boost the convergence rate of digital background calibration for pipelined analog-to-digital converters (ADC). The technique is used to compensate for most known errors, including nonlinear OpAmp gain imperfections, capacitor mismatch and comparator offset. A 12-bit ADC Simulink model is established to verify the technique. Convergence occurs after 5.8K cycle with 42% enhancement over fixed step size LMS. A 22.6% power reduction is achieved as a result of calculation reduction. The proposed technique exhibits improvements in peak DNL from 1 to 0.7 LSB and INL from 33.2 to 2.3 LSB. At a frequency of 100 Msample/s, both SFDR and SNDR reveal noticeable enhancements from 41.6 to 83.1 dB and from 39 to 68.6dB respectively.