Abstract

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Adaptive Power-Efficient Background Calibration Technique for Digitally Assisted Pipelined ADCs

With the rapid increase in the sampling rate, performance and complexity of portable devices, power reduction has become today's number one target. Digital designs benefit from technology scaling that causes significant power and area reduction. In contrast, their analog counterparts have been struggling to maintain their performance at reasonable power dissipation. Scaling makes power-mismatch and power-linearity tradeoffs more challenging in analog-to-digital converter (ADC) implementation. Hence, it demands more complicated power-hungry circuits. Consequently, digital help is needed to relax the analog circuits' specifications as well as to make use of technology scaling. For this reason, digitally-assisted pipelined ADCs are utilized to overcome factors such as capacitor mismatch, limited residue gain and OpAmp nonlinearity, which obviously deteriorate the pipelined ADC performance. This dissertation explores the usage of background digital calibration technique for compensating the pipelined ADCs non-idealities. This technique is capable of tracking system variations continuously without interrupting the conversion process. Equalization-based background technique using least mean squares (LMS) adaptive scheme is presented. Variable step size algorithm (VSS-LMS) is deployed to boost the system convergence. Different VSS-LMS prototypes are investigated and their performances in terms of convergence rate and computational effort are compared to standard LMS. Signed variable step size technique (SVSS) proves to have the highest convergence rate with the least computational effort. Furthermore, dynamic and static ADC performance metrics are evaluated for the proposed calibration technique.