# Abstract


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### Design and Efficient Hardware Implementation for DVB-T2 Modules


DVB-T2 (The second generation Digital Video Broadcasting) is a system enhancement compared to the DVB-T system. The main motivation of DVB-T2 is to provide broadcasters with more reliable, advanced and efficient alternative to DVB-T standard. The cyclic Q delay, cell interleaver and time interleaver are optional modules employed in the DVB-T2 system. The main purpose of these modules is to increase the overall performance of the DVB-T2 system. The cell mapper module is used to build the T2 frames and hence the T2 super frames. The frequency interleaver module which applies a permutation to the T2 frames is employed in the system to increase the ability of data recovery when faces the channel noise. Combining Cyclic Q delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules into one single module is the thesis goal. The combination is to decrease the system complexity, hardware usage and the overall system delay and hence increase the overall DVB-T2 system performance. In this thesis we propose a new module to combine these modules. The new module is simulated and hardware implemented.