Abstract

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Generic FPGA Architecture for Fast Search Block-Based Motion Estimation Algorithm

A design proposal for generic FPGA architecture for fast search block-based motion estimation algorithm is presented. The proposed design can be used in many fast search algorithms such as three step search, diamond search, and hexagon search. Traditionally fast search motion estimation algorithms are well know for their irregularities and inefficient use of parallelism and pipelining compared to full search motion estimation algorithm. The proposed design divides the fast search block matching algorithm into irregular and regular sections. The irregular section is implemented using an algorithm state machine and can vary from one algorithm to another. The regular part is designed using efficient parallelism and pipelining technique that reduces data loading and transfer overhead through a dynamic hardware reconfiguration employed each search iteration using simple control hardware unit.