Abstract

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Design of an 8-bit Pipelined ADC with Lower than 0.5 LSB DNL and INL without Calibration

This paper describes the design of an 8-bit fully differential pipelined analog-to-digital converter (ADC). The design methodology employed in this work follows a technique of allocating appropriate error budgets to the various ADC errors such that the maximum differential nonlinearity (DNL) error is less than 0.5 least significant bits (LSB). Simulation results show that the ADC maximum DNL errors are +0.3/?0.45 LSB, and maximum integral nonlinearity (INL) errors are +0.3/?0.35 LSB. These low figures of nonlinearity errors are achieved without applying any calibration techniques. Simulation also shows an ADC power consumption of only 1.32 mW for a 1.2 V supply, an effective number of bits (ENOB) of 7.94 bits and a figure of merit (FOM) of 2.63 pJ. The pipelined ADC is designed in a 0.13 ?m CMOS process, resulting in a very small active area of 161 ?m × 139 ?m