Abstract

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Effective Scheduling of Semiconductor Manufacturing using Simulation

The process of wafer fabrication is arguably the most technologically complex and capital intensive stage in semiconductor manufacturing. This large-scale discrete-event process is highly reentrant, and involves hundreds of machines, restrictions, and processing steps. Therefore, production control of wafer fabrication facilities (fab), specifically scheduling, is one of the most challenging problems that this industry faces. Dispatching rules have been extensively applied to the scheduling problems in semiconductor manufacturing. Moreover, lot release policies are commonly used in this manufacturing setting to further improve the performance of such systems and reduce its inherent variability. In this work, simulation is used in the scheduling of re-entrant flow shop manufacturing systems with an application in semiconductor wafer fabrication where, a simulation model has been developed for the Intel Five-Machine Six Step Mini-Fab using the ExtendTM simulation environment. The Mini-Fab has been ed as it captures the challenges involved in scheduling the highly re-entrant semiconductor manufacturing lines. A number of scenarios have been developed and have been used to evaluate the effect of different dispatching rules and lot release policies on the ed performance measures. Results of simulation showed that the performance of the Mini-Fab can be drastically improved using a combination of dispatching rules and lot release policy.