Abstract

Ingy A El-Khouly

A Simulation Study of Lot Flow Control in Wafer Fabrication Facilities

The process of wafer fabrication is arguably the most technologically complex stage in semiconductor manufacturing. This manufacturing environment has a number of unusual features. Probably reentrancy of lots and unbalanced production facilities are two of the most important and unique features of semiconductor wafer fabrication facilities (fabs) that necessitate lot flow control and effective scheduling. Lot flow control is achieved by a fixed lot release policy which specifies when new lots are to be released into the fab. Previous studies on a small size fab showed that flow control combined with scheduling results in high throughput, low cycle times, and low work-in-process levels. This work presents a simulation study that has been done for a ed segment in a representative wafer fabrication facility. This segment captures the challenges involved in scheduling the highly re-entrant semiconductor manufacturing lines. A number of scenarios have been developed and are used to evaluate the effect of introducing different input values on the ed performance measures to the best modeling technique.