

Abstract

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Investigation of WIP Management for Control of Semiconductor Manufacturing Segments

The process of wafer fabrication is arguably the most technologically complex stage in semiconductor manufacturing. This manufacturing environment has a number of unusual features. Probably re-entrancy of lots and unbalanced production facilities are two of the most important and unique features of semiconductor wafer fabrication facilities (fabs) that necessitate lot flow control and effective scheduling. Flow control is achieved by a lot release control strategy which specifies when new lots are to be released into the fab. This work starts with analysing the effect of controlling lot releases on a set of performance metrics. Most popular push and pull control strategies were first used to control lot releases in the Intel Five Machine Six Step Minifab. Then a representative segment of an existing wafer fabrication facility operating with the latest technologies used in the semiconductor manufacturing, which captures the challenges involved in scheduling these complex manufacturing systems. Afterwards, based on review of literature and a classification of lot release control strategies, different lot release control strategies were Selected and tested to evaluate and compare their effect on the performance metrics. These tests were conducted using simulation models that have been developed for both the Minifab and the representative segment. Results of the simulation study has shown that pull lot release control strategies can achieve same throughput rate with lower cycle times and work-in-process (WIP) levels compared to traditional push systems. However, further analysis of arrivals variability and WIP distribution has shown that the performance metrics can be further improved by reducing the variability of arrivals this is done by modifying the CONWIP to control the release of lots into the model and reduce the interarrival variability (ICONWIP). Moreover, further analysis showed that application of these strategies lead to unbalanced distribution of WIP across the segment. To address this, a Looped CONWIP (LCONWIP)strategy which balances this load by looking the WIP in each re-entrant loop, was developed. This improves the performance while maintaining a balanced load across the line. The results of the simulation have shown that ICONWIP outperforms both LCONWIP and the traditional CONWIP at reducing the WIP levels and cycle times.