

Abstract

Fadi S Ayad

Design and Implementation of a Real-time Sleep Stage Monitoring System for Narcolepsy Diagnosis

A number of illnesses that affect people's daily life are caused by numerous sleep disorders which usually have common symptoms. People suffering from such illnesses are more vulnerable to household and work accidents. While there is no treatment for these kinds of neurological disorders, symptoms can be managed with behavioral and medical therapies to reduce the intensity and occurrence rates. The scope of this thesis is to design and implement a portable system that will assist Narcoleptic patients, in real-time, to aid them into leading a more productive life. The system consists of two main units, a feature extraction unit based on the Wavelet Packet Transforms (WPT), and a classification unit based on the Support Vector Machine (SVM) algorithm. The SVM used is a non-linear and multi-class classification using the Radial Basis Function (RBF) as the kernel function. The design undergoes two testing processes, the first one is a software simulation using MATLAB 2014a tool, while the second is the RTL simulation using ModelSim 6.3a. The hardware RTL simulation is compared to the software simulation to determine the average error of the feature extraction unit, and the classifier accuracy. The feature extraction unit achieved an average percentage of error 0.1618% with respect to the software simulation, while the classifier achieved an average accuracy rate of 92.14% and 90.5% by software and the RTL simulations respectively. The design is synthesized and routed – using Quartus II V. 13 – on Cyclone IV EP4CGX30BF14C6 chip from Altera. The gate level simulation resulted with the same results as the RTL simulation. The implementation achieved an acceptable time delay, where the feature extraction and the classification are executed in 3.85ms. The total area usage of the Selected FPGA chip is 97.68% of the available logic elements, 8.42% of the available memory bits, and 32.5% of the available embedded multiplier units.