

# Abstract

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## **Design and Implementation of a Video Compression technique for HD videos on FPGA**

High definition videos contain huge data to be transmitted &#97;&#110;&#100; received, which is difficult to be sent &#97;&#110;&#100; stored. In this paper a compression technique based on binary motion vector technique is used to compress HD videos. In which the process of searching for the best matching block for each current block occurs. The proposed technique keeps HD quality with at least Peak Signal to Noise Ratio 62 dB &#97;&#110;&#100; along with 26% compression ratio on gray scale. The proposed technique is implemented on a Xilinx Vertex 2 2V250fg456 FPGA. The maximum operating speed of the hardware is 63.8 MHz. The FPGA utilization is 12.37% of total CLB slices &#97;&#110;&#100; 8.61% of total latches.