Abstract

Design and implementation of soft Decision Low Density Parity check decoder (LDPC) on Field Programmable Gate Array (FPGA)

The Low-Density Parity-Check (LDPC) codes are among the most powerful forward error correcting codes. LDPC codes enable performance close to the Shannon limit. This advantage combined with their relatively simple decoding algorithm makes these codes very attractive for the second digital transmission system generations. It is already the case for the next digital satellite broadcasting standard (DVB-S2). Thesis proposes two different LDPC algorithms named Log-BP and MS. Both of them are software implemented using Matlab m-files. They are analysed to compare between their performance. The analysis is performed on two different channels named AWGN and Rayleigh fading channels. The choice for this channels to study the performance of LDPC decoders in different environments as AWGN channel is considered to be an ideal while the Rayleigh fading channel considered to be practical channel in daily environment. The MS LDPC decoder is fully parallel implemented on LabVIEW which is a semi Hardware simulation tool. Afterwards using the same MS LDPC decoder but using partially parallel architecture implemented on VHDL hardware simulation tool. The used EDA tools is Mentor Graphics FPGA adv. prog.8.2. The partial parallel architecture is used to enhance the performance of the design while saving hardware area. It is a compromise between speed and area performance. The implemented decoder results are verified by a successful comparison with the simulated one. The decoder The Low-Density Parity-Check (LDPC) codes are among the most powerful forward error correcting codes. LDPC codes enable performance close to the Shannon limit. This advantage combined with their relatively simple decoding algorithm makes these codes very attractive for the second digital transmission system generations. It is already the case for the next digital satellite broadcasting standard (DVB-S2). Thesis proposes two different LDPC algorithms named Log-BP and MS. Both of them are software implemented using Matlab m-files. They are analysed to compare between their performance. The analysis is performed on two different channels named AWGN and Rayleigh fading channels. The choice for this channels to study the performance of LDPC decoders in different environments as AWGN channel is considered to be an ideal while the Rayleigh fading channel considered to be practical channel in daily environment. The MS LDPC decoder is fully parallel implemented on LabVIEW which is a semi Hardware simulation tool. Afterwards using the same MS LDPC decoder but using partially parallel architecture implemented on VHDL hardware simulation tool. The used EDA tools is Mentor Graphics FPGA adv. prog.8.2. The partial parallel architecture is used to enhance the performance of the design while saving hardware area. It is a compromise between speed and area performance. The implemented decoder results are verified by a successful comparison with the simulated one. The decoder The Low-Density Parity-Check (LDPC) codes are among the most powerful forward error correcting codes. LDPC codes enable performance close to the Shannon limit. This advantage combined with their relatively simple decoding algorithm makes these codes very attractive for the second digital transmission system generations. It is already the case for the next digital satellite broadcasting standard (DVB-S2). Thesis proposes two different LDPC algorithms named Log-BP and MS. Both of them are software implemented using Matlab m-files. They are analysed to compare between their performance. The analysis is performed on two different channels named AWGN and Rayleigh fading channels. The choice for this channels to study the performance of LDPC decoders in different environments as AWGN channel is considered to be an ideal while the Rayleigh fading channel considered to be practical channel in daily environment. The MS LDPC decoder is fully parallel implemented on LabVIEW which is a semi Hardware simulation tool. Afterwards using the same MS LDPC decoder but using partially parallel architecture implemented on VHDL hardware simulation tool. The used EDA tools is Mentor Graphics FPGA adv. prog.8.2. The partial parallel architecture is used to enhance the performance of the design while saving hardware area. It is a compromise between speed and area performance. The implemented decoder results are verified by a successful comparison with the simulated one. The decoder The

Low-Density Parity-Check (LDPC) codes are among the most powerful forward error correcting codes. LDPC codes enable performance close to the Shannon limit. This advantage combined with their relatively simple decoding algorithm makes these codes very attractive for the second digital transmission system generations. It is already the case for the next digital satellite broadcasting standard (DVB-S2). Thesis proposes two different LDPC algorithms named Log-BP and MS. Both of them are software implemented using Matlab m-files. They are analysed to compare between their performance. The analysis is performed on two different channels named AWGN and Rayleigh fading channels. The choice for this channels to study the performance of LDPC decoders in different environments as AWGN channel is considered to be an ideal while the Rayleigh fading channel considered to be practical channel in daily environment. The MS LDPC decoder is fully parallel implemented on LabVIEW which is a semi Hardware simulation tool. Afterwards using the same MS LDPC decoder but using partially parallel architecture implemented on VHDL hardware simulation tool. The used EDA tools is Mentor Graphics FPGA adv. prog.8.2. The partial parallel architecture is used to enhance the performance of the design while saving hardware area. It is a compromise between speed and area performance. The implemented decoder results are verified by a successful comparison with the simulated one. The decoder is then synthesized proving hardware realization.