Design of an 8-bit Pipelined ADC with Lower than 0.5 LSB DNL and INL without Calibration

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***Abstract*—This paper describes the design of an 8-bit fully differential pipelined analog-to-digital converter (ADC). The design methodology employed in this work follows a technique of allocating appropriate error budgets to the various ADC errors such that the maximum differential nonlinearity (DNL) error is less than 0.5 least significant bits (LSB). Simulation results show that the ADC maximum DNL errors are +0.3/-0.45 LSB, and maximum integral nonlinearity (INL) errors are +0.3/-0.35 LSB. These low figures of nonlinearity errors are achieved without applying any calibration techniques. Simulation also shows an ADC power consumption of only 1.32 mW for a 1.2 V supply, an effective number of bits (ENOB) of 7.94 bits and a figure of merit (FOM) of 2.63 pJ. The pipelined ADC is designed in a 0.13 µm CMOS process, resulting in a very small active area of 161 µm × 139 µm.**

Keywords-component; Pipelined analog-to-digital converter (ADC); DNL; INL, low nonlinearity errors; design methodology.

I. INTRODUCTION

The vast majority of signal processing is done digitally. Since signals in nature are analog, analog–to-digital converters (ADCs) are required to convert these analog signals into digital so they can be processed by the digital signal processors. Also, there is an increasing demand on wireless devices and on converting non-wireless devices into wireless. These wireless devices must have ADCs to receive the transmitted wireless signals. For these reasons, ADCs are fundamental building block in today's integrated circuits (ICs). This led to the increase in research activities to improve the ADCs performance, which is very challenging particularly in the modern low-voltage deep submicron fabrication technologies.

The pipelined ADC is one of the most common ADC architectures. This is because it can achieve high resolutions and conversion rates, while having intermediate power consumption. Factors such as nonlinearity errors and noise degrade the ADC resolution. Therefore, the true ADC resolution is usually less than the designed resolution. This true resolution is known as the effective number of bits (ENOB), which is calculated after taking into consideration all distortions and noise sources types. Having an ENOB lower than the designed ADC resolution indicates that some of the least significant bits (LSBs) are inaccurate [1].

This paper presents the design of an 8-bit ADC, following a design methodology to limit the maximum differential nonlinearity (DNL) error and circuit noise in order to increase the ENOB. The paper is organized into an introduction, five sections and a conclusion. Section II describes details of the pipelined ADC's system architecture and circuit design. Section III presents the followed design methodology and the design considerations taken into account during the design of the ADC. In Section IV, the pipelined ADC simulation results are shown. Section V presents the proposed layout of the designed pipelined ADC.

II. SYSTEM DESIGN AND ARCHITECTURE

A. Pipelined ADC Architecture

The block diagram of the designed 8-bit pipelined ADC is shown in Figure 1. It consists of an input sample-and-hold amplifier (SHA) stage, eight sub-converter stages, a time alignment block and a digital error correction (DEC) block. Each of the first seven stages consists of a multiplying digital-to-analog converter (MDAC) and a sub-ADC, while the last stage consists of only a sub-ADC.

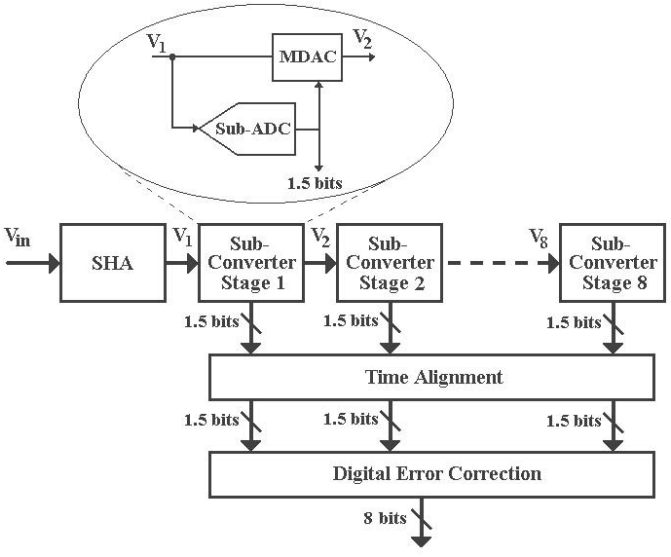

Figure 1. Designed pipelined ADC block diagram.

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Each of the sub-ADCs is designed to resolve 1.5 bits/stage which is the least possible value. This decision is taken for the following reasons:

i) A closed-loop gain of two is required in the MDAC circuit. This is achieved when the sampling capacitors of the MDAC circuit are equal, which leads to best probability of matching between the capacitors [2]. This reduces the probability of having nonlinearity errors due to capacitor mismatches.
ii) The DEC range of error correction for comparator offsets in the sub-ADC is maximized. This greatly relaxes the comparator accuracy requirement, and so allows the use of simple comparators which dissipate less power and occupy smaller die area [3]–[5].
iii) The closed-loop MDAC circuit gain is minimized, which maximizes the closed-loop bandwidth of the MDAC circuit, resulting in a higher conversion rate [4], [5].

B. Sample-and-Hold Amplifier (SHA)

The differential unity-gain SHA [6] circuit is designed using the flip-around capacitor circuit architecture, shown in Figure 2. The SHA operation is controlled by the three clock signals (ϕ_1, ϕ_1' and ϕ_2) shown in Figure 3.

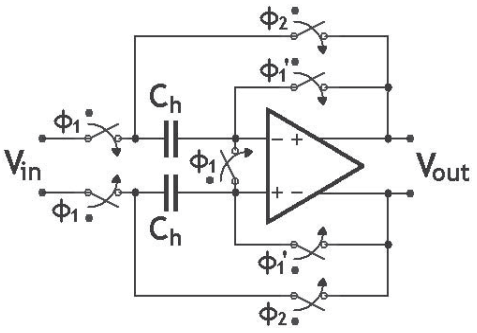

Figure 2. Designed SHA circuit.

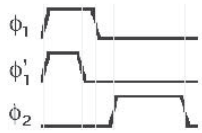

Figure 3. SHA circuit clock waveforms.

C. Multiplying Digital-to-Analog Converter (MDAC)

The MDAC architecture used is the switched capacitor (SC) MDAC using a flip-around capacitor as illustrated in Figure 4. The SC MDAC topology is chosen rather than the switched op-amp MDAC topology for its ability to operate at higher speeds [5]. The MDAC circuit is controlled by the same clock signals (ϕ_1, ϕ_1' and ϕ_2) controlling the SHA.

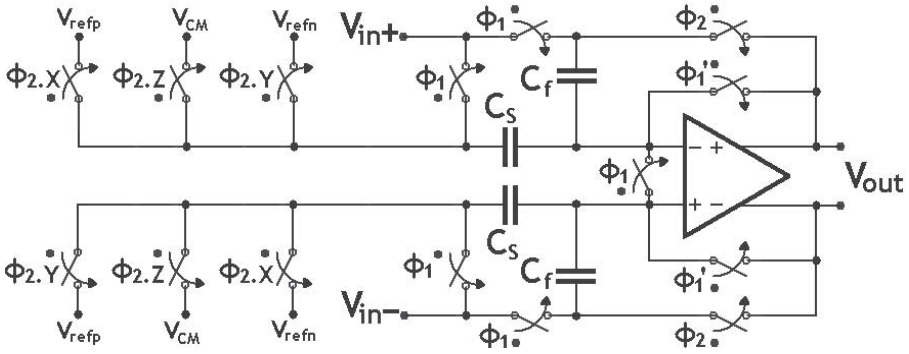

Figure 4. Designed MDAC circuit.

D. Sub-ADC

The sub-ADC of each stage of the pipelined ADC is a low resolution flash ADC, as shown in Figure 5. The sub-ADC has a differential operation as the differential comparators used to implement it. Each sub-ADC has only two differential comparators with their thresholds at $\pm V_{ref}/4$, where $+V_{ref}$ and $-V_{ref}$ are respectively the maximum and minimum ADC input differential voltages.

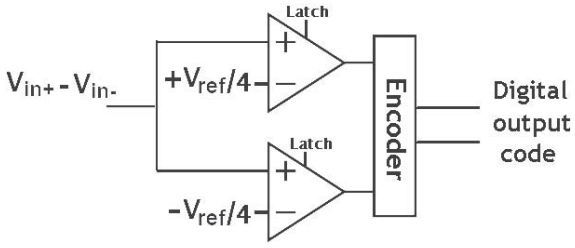

Figure 5. Sub-ADC circuit.

E. Operational Amplifier

The differential folded-cascode topology is used in designing the operational amplifier (op-amp) shown in Figure 6. This topology is chosen for its ability to operate at high speeds and because it allows the short-circuiting of its input and output terminals [7].

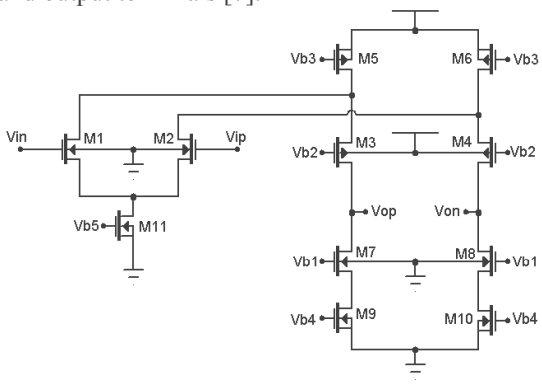

Figure 6. Folded-cascode op-amp circuit.

The op-amps are the main source of power dissipation in the pipelined ADC circuit. The power consumption of the ADC is reduced by reducing the power dissipation of the op-amps. This is done by designing the op-amps to achieve high gain without using gain boosting techniques. The designed op-amp simulated power dissipation is found to be only 146 μW.

F. Comparator

The comparators used in the sub-ADC circuit are latched differential comparators [8]. The topology used in designing the latched comparator circuit is the resistive divider topology [9], shown in Figure 7.

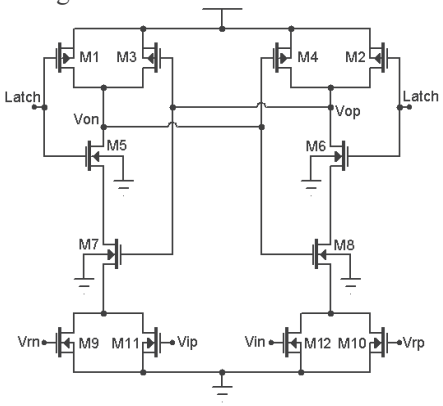

Figure 7. Comparator circuit.

The main advantages of this comparator architecture compared to other architectures are the low power consumption due to no static power dissipation, and the possibility of adjusting the comparator's threshold. To adjust the comparator's threshold, the ratios between the channel widths of the input transistors (*M9, M10, M11* and *M12*) are adjusted while keeping their channel lengths constant. The comparator threshold is given by (1) [8].

$$\frac{W_a}{W_b} = \frac{Vip - Vin}{Vrp - Vrn} \tag{1}$$

Where W_a is the channel width of transistors *M9* and *M10*, W_b is the channel width of transistors *M11* and *M12*, *Vip* and *Vin* are the comparator's differential input signal, and *Vrp* and *Vrn* are the comparator's differential reference signal.

Equation (1) is advantageously exploited to avoid using resistor ladders to generate the comparators' threshold voltages ($V_{ref}/4$ and $-V_{ref}/4$) of the sub-ADC circuit. The disadvantages of using resistor ladders are the requirement for a large area, dissipation of power, and inaccurate generation of the threshold voltage values in low cost fabrication processes. To avoid these disadvantages, voltages V_{ref} and $-V_{ref}$ are connected to the comparators' inputs and the comparators' thresholds are adjusted to 0.25 by making W_a/W_b equal to 0.25. This threshold shift is equivalent to connecting $V_{ref}/4$ and $-V_{ref}/4$ to the comparators inputs.

III. Circuit Design Methodology and Considerations

Non-ideal factors degrade the ideal functionality of the SHA and MDAC circuits leading to an increase in the ADC nonlinearity errors and circuit noise, and therefore the final resolution and conversion rate of the ADC are limited. Significant non-ideal factors include the switching charge injection, thermal noise, and op-amp finite open-loop gain, input parasitic capacitance and output voltage settling error.

In the design of the pipelined ADC, error budgets are allocated to the different errors due to the non-ideal factors. The sum of all error budgets should lead to nonlinearity errors of maximum 0.5 LSB in the ADC output. In pipelined ADCs, it is difficult to analyze the anticipated integral nonlinearity (INL) error due to the nonlinearity of the residue transfer function [10]. For this reason, only DNL is analyzed.

A. Switching Charge Injection Distortion

As the transmission gates in the SHA and MDAC circuits are switched 'OFF', charges are injected from the transistors parasitic capacitances onto the sampling capacitors. These injected charges add an error voltage to the voltage across the capacitors. The charge injected (Q) by each of the PMOS and NMOS transistors of the transmission gate is given by (2) [11].

$$Q = WLC_{ox}(V_{gs} - V_t) \tag{2}$$

Where W, L, C_{ox}, V_{gs} and V_t are respectively the transistor channel width, channel length, gate oxide capacitance, gate-to-source voltage and threshold voltage.

The transmission gate transistors are designed with minimum channel length and width to reduce the injected charges and clock feed-through. Furthermore, all the pipelined ADC analog circuit architectures are designed fully differential. This is because the voltage error due to charge injections of the switches is insignificant in differential circuits, due to its negligible effect to the first order. This is because the added voltage error is a common-mode noise. Equal voltages are added to both positive and negative sides of the designed differential circuits, and so they cancel each other in the circuits outputs [5], [8].

B. Thermal Noise Distortion

Calculating the circuits thermal noise is an important step in the pipelined ADC design. It determines the MDAC and SHA minimum sampling capacitors values. As the op-amp capacitance load value decreases, the op-amp slew rate and bandwidth increase, and so does the ADC maximum conversion rate. On the other hand, by decreasing the capacitance load value, the voltage thermal noise on the capacitors increases. If this noise exceeds or is approximately equal to the quantization noise, then the SNR and ENOB will decrease noticeably. It is required to select values for the sampling capacitors that will not noticeably degrade the SNR and ENOB, and would still allow a high conversion rate.

The noise in any stage of the pipelined ADC includes the accumulated thermal noise from all the previous stages. The thermal noise in all stages is uncorrelated. The pipelined ADC input-referred accumulated thermal noise power (v^2_{ni}) is calculated using (3) [12].

$$v^2_{ni} = v^2_{n,SHA} + v^2_{n,MDAC1} + \frac{v^2_{n,MDAC2}}{G_1^2} + \frac{v^2_{n,MDAC3}}{G_1^2 . G_2^2} + ... \tag{3}$$

Where $v^2_{n,SHA}$ is the output thermal noise power of the SHA, $v^2_{n,MDAC,i}$ is the output thermal noise power of the MDAC from sub-converter stage i, and G_i is the closed-loop gain of

sub-converter stage *i*. G_i is equal to two for the implemented 1.5 bits/stage pipelined ADC structure. It can be shown that the input-referred thermal noise powers of the SHA and MDAC are given by (4) and (5), respectively.

$$v_{n,SHA}^2 = 2\frac{k_B T}{C_h} + v_{n,op-amp}^2 + 8k_B T R_{on} B_{eq} \quad (4)$$

$$v_{n,MDAC,i}^2 = \left(4\frac{k_B T}{C_f} + v_{n,op-amp}^2 + 16k_B T R_{on} B_{eq}\right)\frac{1}{G_i^2} \quad (5)$$

Where k_B is the Boltzmann constant, T is the absolute temperature, $v^2_{n,op\text{-}amp}$ is the thermal noise power due to the op-amp, R_{on} is the transmission gate 'ON' resistance, B_{eq} is the noise bandwidth by the op-amp, C_h is the SHA sampling capacitor, and C_f is the MDAC feedback sampling capacitor.

The op-amp thermal noise is given by (6) [7], and the noise bandwidth is given by (7) [13].

$$v_{n,op-amp}^2 = \frac{16}{3}\frac{k_B T}{g_{m1}}\left(1 + \frac{g_{m5} + g_{m9}}{g_{m1}}\right)B_{eq} \quad (6)$$

$$B_{eq} = \frac{\pi}{2} f_{CL} \quad (7)$$

In (6) and (7) above, f_{CL} is the op-amp closed-loop bandwidth and g_{mi} is the transconductance of the op-amp transistor *i*, as shown in Figure 6.

The ADC expected thermal noise power is estimated from the set of equations, (3) - (7), described above. The thermal noise power is considered of an acceptable value when it is lower than the quantization noise power. In case the noise power is equal to the quantization noise, then the SNR will decrease by 3 dB [13]. For Nyquist sampling rate ADCs, the quantization noise power is given by (8) [14].

$$P_Q = \frac{1}{12}.\left(\frac{FSR}{2^N}\right)^2 \quad (8)$$

The SHA stage circuit is responsible for most of the thermal noise power, while the rest of the stages contribute with only a small portion. This is because the input-referred noise power is divided by the MDAC circuit gain squared after each MDAC stage, which makes the last stages in the pipelined ADC have a negligible contribution to the noise power. The large thermal noise power from the SHA could limit the maximum possible ADC resolution. Some pipelined ADCs are implemented without a dedicated SHA to reduce the power consumption and total thermal noise. This is done by integrating the pipelined ADC front-end SHA into the first sub-converter stage [15].

C. Op-amp Finite Gain and Input Capacitance

The op-amp is the most critical block in the pipelined ADC. Its performance directly affects the SHA and MDAC transfer functions and their output settling voltages, which could lead to an unacceptable level of nonlinearity errors in the pipelined ADC output. It is required to determine the maximum DNL error output from the pipelined ADC due to the op-amp finite open-loop gain and input parasitic capacitance.

For the used 1.5 bits/stage MDAC structure, the transfer function including the effects of the op-amp finite open-loop gain and input parasitic capacitance is given by (9) - (11) [14].

$$V_{o,MDAC} = \left(\left(1 + \frac{C_s}{C_f}\right)V_i + \left(\frac{C_s}{C_f}\right)V_{ref}\right)\left(1 - \frac{2}{a} - \frac{C_p}{aC_f}\right) \quad \text{, for } -V_{ref} < V_i < -V_{ref}/4 \quad (9)$$

$$V_{o,MDAC} = \left(\left(1 + \frac{C_s}{C_f}\right)V_i\right)\left(1 - \frac{2}{a} - \frac{C_p}{aC_f}\right) \quad \text{, for } -V_{ref}/4 \le V_i \le V_{ref}/4 \quad (10)$$

$$V_{o,MDAC} = \left(\left(1 + \frac{C_s}{C_f}\right)V_i - \left(\frac{C_s}{C_f}\right)V_{ref}\right)\left(1 - \frac{2}{a} - \frac{C_p}{aC_f}\right) \quad \text{, for } V_{ref}/4 < V_i < V_{ref} \quad (11)$$

In (9) – (11) above, C_s and C_f are the MDAC's sampling capacitors, C_p is the op-amp's input parasitic capacitance, and a is the op-amp's DC open-loop gain.

Equation (12) [6] gives the SHA output voltage including the effects of the op-amp finite open-loop gain and input parasitic capacitance.

$$V_{o,SHA} = V_i \times \left(1 - \frac{1}{a} - \frac{C_p}{aC_h}\right) \quad (12)$$

The voltage error after each stage due to the op-amp finite open-loop gain and input parasitic capacitance is correlated. This makes the total error after stage *i* equal to the linear summation of all the errors from previous stages. The pipelined ADC input-referred accumulated voltage error (v_{ei}) is given by (13) [13], [14].

$$v_{ei} = v_{e,SHA} + v_{e,MDAC1} + \frac{v_{e,MDAC2}}{G_1} + \frac{v_{e,MDAC3}}{G_1.G_2} + ... \quad (13)$$

In (13) above, $v_{e,SHA}$ is the op-amp output voltage error of the SHA, and $v_{e,MDAC,i}$ is the op-amp output voltage error of the MDAC in sub-converter stage *i*.

The maximum input-referred voltage values for $v_{e,SHA}$ and $v_{e.MDAC,i}$ are given by (14) and (15), respectively [6], [14].

$$v_{e,SHA,\max} = V_{ref}\left(\frac{1}{a}+\frac{C_p}{aC_h}\right) \quad (14)$$

$$v_{e,MDAC,i,\max} = \frac{1}{2}V_{ref}\left(\frac{2}{a}+\frac{C_p}{aC_f}\right) \quad (15)$$

The maximum error output from the pipelined ADC due to the op-amp finite open-loop gain and input parasitic capacitance is estimated from the set of equations, (13) - (15), described above.

D. Op-amp Output Voltage Settling Error

After estimating the error due to the op-amp finite open-loop gain and input parasitic capacitance, the error budget left for assignment to other errors types for a maximum DNL error of 0.5 LSB in the ADC output is estimated. The remaining error budget is assigned to the settling voltage errors in the op-amps outputs from the different stages of the pipelined ADC. It is required to determine the minimum settling time for the op-amps output voltages to settle within the specified accuracy of the assigned error budget. By determining the op-amps minimum settling time ($T_{Settling}$), the pipelined ADC maximum conversion rate (F_s) is calculated using (16).

$$F_s = \frac{1}{2.T_{Settling}} \quad (16)$$

For an op-amp to settle with a fraction accuracy equals to ε_{LSB} from the LSB in an N-bit system, the minimum number of time constants (N_T) required for a first order op-amp settling can be shown to be given by (17).

$$N_T = \ln\left(\frac{2^N}{2(\varepsilon_{LSB})}\right) \quad (17)$$

The minimum settling time for a first order op-amp settling taking into consideration the slew rate is given by (18) [12].

$$T_{Settling} \geq \frac{N_T}{\omega_{CL}} + T_{SR} \quad (18)$$

Where T_{SR} is the op-amp slewing time and ω_{CL} is the op-amp closed-loop dominant pole frequency.

For differential op-amps, T_{SR} is calculated using (19).

$$T_{SR} = \frac{FSR}{2.SR} \quad (19)$$

Due to the correlation between op-amps' output voltage settling errors from the different stages, (13) is used to calculate the input-referred accumulated error at the ADC output resulting from all the op-amps settling errors [14].

The pipelined ADC maximum conversion rate is estimated for a maximum DNL error of 0.5 LSB using the set of equations, (13) -(19),described above.

IV. Simulation Results

The complete circuit design of the pipelined ADC is simulated for an input ramp signal rising from $-V_{ref}$ to V_{ref}. The output bits are processed to obtain the various ADC performance parameters.

Figure 8 shows the simulated DNL and INL errors for the different output digital codes. The maximum DNL errors are +0.3/-0.45 LSB and the maximum INL errors are +0.3/-0.35 LSB.

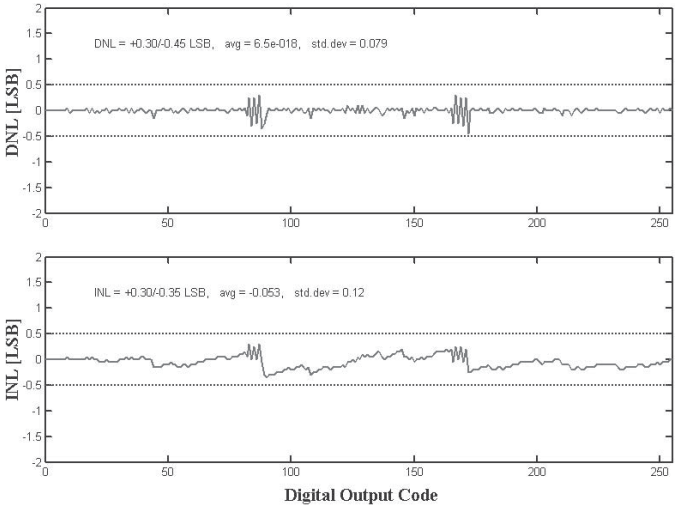

Figure 8. Designed pipelined ADC simulated DNL and INL errors.

A 3181-cycle sinusoidal signal with a peak voltage of V_{ref} and a frequency (f_{in}) of 97 kHz is quantized with the pipelined ADC simulated thresholds levels. Then, Fast Fourier Transform (FFT) is applied to this signal in order to analyse its frequency spectrum. Figure 9 shows the expected pipelined ADC output frequency spectrum for the input of the sinusoidal signal. The signal to noise ratio (SNR), total harmonic distortion (THD), signal to noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR) and effective number of bits (ENOB) are found to be 49.7 dB, -66.7 dB, 49.6 dB, 67.0 dB and 7.94 bits, respectively.

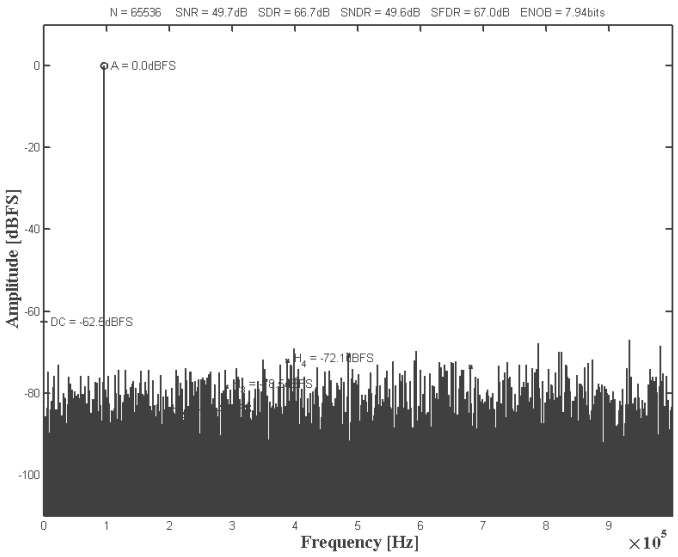

Figure 9. Designed pipelined ADC simulated output frequency spectrum for a sinusoidal signal input of 97 kHz.

V. Layout

The pipelined ADC is designed using a standard 0.13 µm CMOS technology. The layout of the active area is shown in Figure 10. The resulting size of the active area is small, approximately 161 µm × 139 µm. Table 1 summarizes the performance parameters of the designed 8-bit pipelined ADC.

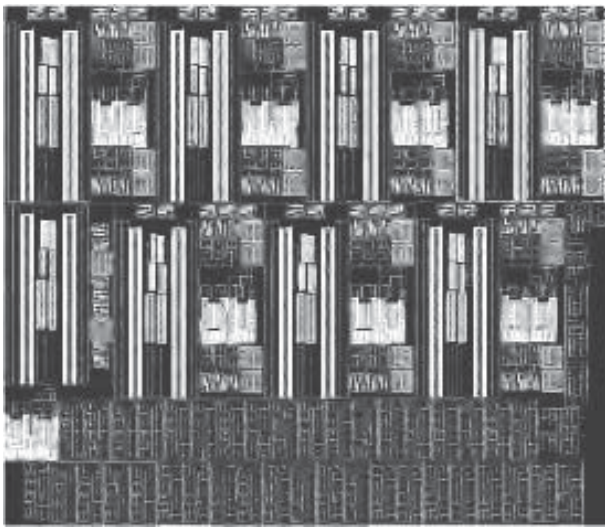

Figure 10. Pipelined ADC active area layout.

TABLE I

Summary of ADC Performance Parameters

Technology	CMOS 0.13 µm
Supply voltage	1.2 V
Resolution	8 bits
Conversion rate	2 MS/s
Input swing (differential)	0.54 $V_{p\text{-}p}$
DNL	+0.3/-0.45 LSB
INL	+0.3/-0.35 LSB
SNR* (f_{in} = 97 kHz)	49.7 dB
THD (f_{in} = 97 kHz)	-66.7 dB
SNDR* (f_{in} = 97 kHz)	49.6 dB
SFDR (f_{in} = 97 kHz)	67.0 dB
ENOB* (f_{in} = 97 kHz)	7.94 bits
Input capacitance (per terminal)	100 fF
Power dissipation** (analog / digital)	1.32 mW (1.22 / 0.1 mW)
FOM** $=\left(\frac{power}{2 f_m 2^{ENOB}}\right)$	2.63 pJ
Active area**	161 µm × 139 µm

* Due to thermal noise, this value is estimated to decrease by approximately 1.95 dB or 0.32 LSB.

** Does not include contributions by clock generation, voltage bias generation, and input-output pad circuits.

VI. Conclusion

The design of a fully differential 8-bit pipelined ADC in a 0.13 µm CMOS technology has been presented. The design methodology employed in order to limit the nonlinearity errors in the pipelined ADC output has been described. The ADC simulated maximum DNL and INL errors are +0.3/-0.45 LSB and +0.3/-0.35 LSB, respectively. No calibration techniques were applied in order to achieve these low figures of nonlinearity errors. The simulated pipelined ADC ENOB is found to be 7.94 bits, while the ADC power dissipation is 1.32 mW for a 1.2 V supply, and the resulting Figure of Merit (FOM) is 2.63 pJ. The layout of the active area has been shown, with a resulting size that is as small as approximately 161 µm × 139 µm.

Acknowledgment

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