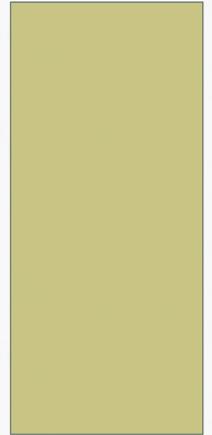


EC233

ELECTRONIC DEVICES 1

SHEET 5 SOLUTIONS



PART I:

TRUE OR FALSE

1. At thermal equilibrium, the total current through a pn junction is zero because the electron current is balanced by the hole current. ❌

2. The built-in potential increases as the doping on both sides of the junction are increased. ✓

$$V_{bi} = \frac{KT}{q} \ln \frac{N_a N_d}{n_i^2}$$

3. The cut-in voltage of diode made of low energy gap semiconductor is higher than that of a diode made of high energy gap semiconductor. ❌

PART I:

TRUE OR FALSE

4. As the temperature is increased, the built-in potential is decreased.

$$V_{bi} = \frac{KT}{q} \ln \frac{N_a N_d}{n_i^2}$$



5. The space-charge (depletion) layer width increases with doping.

$$w = \left[\frac{2\epsilon KT}{q^2} \left(\frac{N_a + N_d}{N_a N_d} \right) \ln \left(\frac{N_a N_d}{n_i^2} \right) \right]^{\frac{1}{2}}$$



6. The electric field in the depletion layer of a pn junction at equilibrium is directed from the n-side to the p-side.



7. As the temperature is lowered, the built-in voltage decreases.



8. For a pn-junction diode at a fixed temperature, the higher is the potential barrier (built-in potential), the lower is the depletion layer width.



$$w = \left[\frac{2\epsilon}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) V_{bi} \right]^{\frac{1}{2}}$$

PART II:

CHOOSE THE CORRECT ANSWER

1- The built-in potential in a pn junction prevents.....

- (a) more holes to diffuse from n-side to p-side
- (b) more electrons to diffuse from p-side to n-side
- (c) more electrons to move from the valence band to the conduction band
- (d) more electrons to diffuse from n-side to p-side

2- The electric field in the depletion layer of a pn junction has an absolute maximum value at

- (a) the p-neutral region
- (b) the n-neutral region
- (c) the metallurgical junction
- (d) the point of highest potential

3- For a pn junction at thermal equilibrium, The electric potential is highest

- (a) in the p-neutral region
- (b) in the n-neutral region
- (c) at the metallurgical junction
- (d) at the point of maximum electric field

PART III: PROBLEMS

1- Consider an abrupt silicon pn junction in which the acceptor concentration is $4 \times 10^{18} \text{ cm}^{-3}$ and the donor concentration is 10^{16} cm^{-3} . Determine the depletion widths for the junction and the maximum electric field at room temperature (300 K) where the relative permittivity of silicon is 11.8.

$$V_{bi} = \frac{KT}{q} \ln \frac{N_a N_d}{n_i^2}$$

$$w = \left[\frac{2\epsilon}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) V_{bi} \right]^{\frac{1}{2}}$$

$$V_{bi} = \frac{1}{2} \epsilon_o w$$

PART III: PROBLEMS

3 - A Si p-n junction has the following : $N_D = 4 \times 10^{24} \text{ m}^{-3}$ in the n-side , $N_A = 2 \times 10^{22} \text{ m}^{-3}$ in the p-side . Calculate the built-in junction voltage and the maximum electric field within the depletion region.