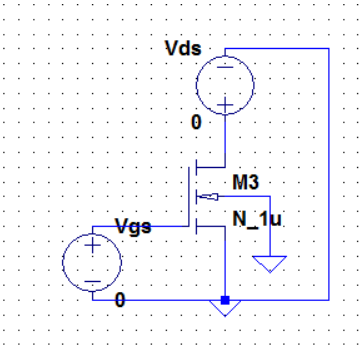
Arab Academy for Science & Technology and Maritime Transport – Cairo Branch
College of Engineering & technology
Electronics & Communication Engineering Department

Course: Selected Topics in Electronics **Course Code**: EC538

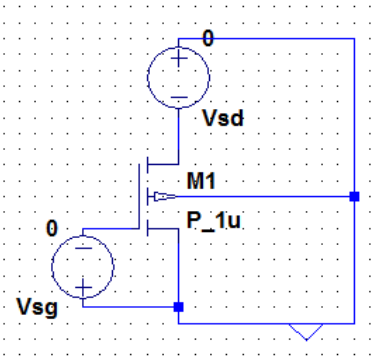
Problem Set

MOSFET I-V Characteristics

P1. Plot the Id-Vds curve with Vgs ranging from 0 to 5 using Level 3 N-MOSFET Model for L=1u and W=10u in cmosedu_models.txt.



P2. Plot the Id-Vsd curve with Vsg ranging 0 to 5 using Level 3 P-MOSFET Model for L=1u and W=10u in cmosedu_models.txt.



P3. Plot the Id-Vds curve with Vgs ranging from 0 to 1 using BSIM4 N-MOSFET Model for L=50n and W=500n in cmosedu_models.txt.

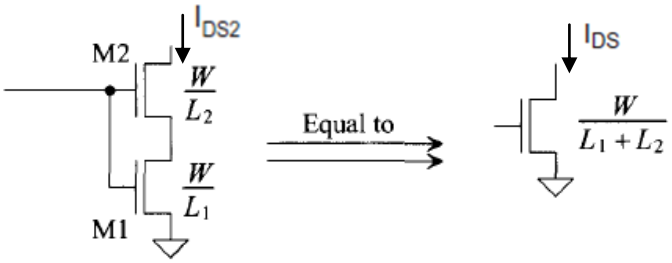
P4. Plot the Id-Vsd curve with Vsg ranging 0 to 1 using BSIM4 P-MOSFET Model for L=50n and W=500n in cmosedu_models.txt.

MOSFET Series/Parallel Configurations

P5. Show that the parallel connection of the MOSFETs shown below behave as a single MOSFET with a width equal to the sum of each individual MOSFET width.

Prove using LTSpice for the Level 3 N-MOSFET Model.

P6. Show that the series connection of MOSFETs shown behaves as a single MOSFET with twice the length of the individual MOSFETs. Neglect the body effect.

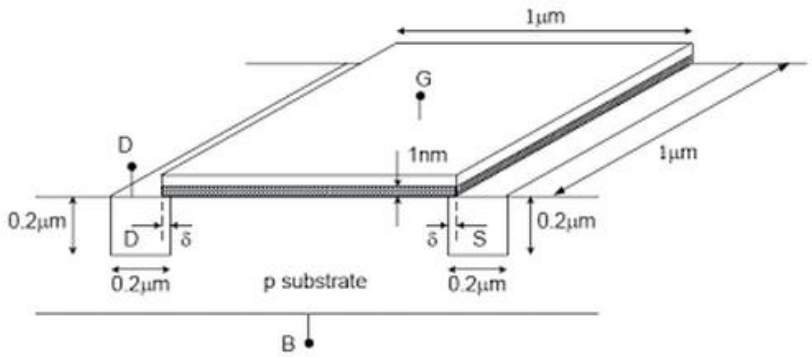


MOSFET Capacitance

P7. A 90 nm long transistor has a gate oxide thickness of 16 Å. What is its gate capacitance per micron of width?

P8. Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted NMOS transistor in a 0.6 μm process if the size of the diffusion contact is 4x5λ when the drain is at 0 and at VDD = 5 V. Assume the substrate is grounded. The transistor characteristics are CJ = 0.42 fF/μm^2, MJ =0.44, CJSW = 0.33 fF/μm, MJSW = 0.12, and ψ_0 = 0.98 V at room temperature.

P9. In the three dimensional view of a silicon n-channel MOS transistor shown below, δ= 20 nm. The transistor is of width 1 μm. The depletion width formed at every p-n junction is 10 nm. The relative permittivity of Si and SiO2 respectively, are 11.7 and 3.9, and Ɛ0 = 8.9 X 10-12F/m. Find the gate source overlap capacitance.



Body Effect

P10. Using LTSpice, for NMOS and PMOS:

(a) Find the value of the threshold voltage if V_{sb}/V_{bs} =0.

(b) Prove that when V_{sb}/V_{bs} is increased, the threshold voltage goes up.

(c) Draw Id versus V_{sb}/V_{bs}.

Compare all of the above using both Level3 and BSIM4 Model cards.

P11. Sometimes the substrate is connected to a voltage called the substrate bias to alter the threshold of the nMOS transistors. If the threshold of an nMOS transistor is to be raised, should a positive or negative substrate bias be used?

P13. Consider the nMOS transistor in a 0.6 μm process with gate oxide thickness of 100 Å. The doping level is NA = 2 × 1017 cm^{-3} and the nominal threshold voltage is 0.7 V. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4 V instead of 0? The intrinsic carrier concentration for Silicon is 1.45x1010cm^{-3} and the relative permittivity for Silicon is 11.7.

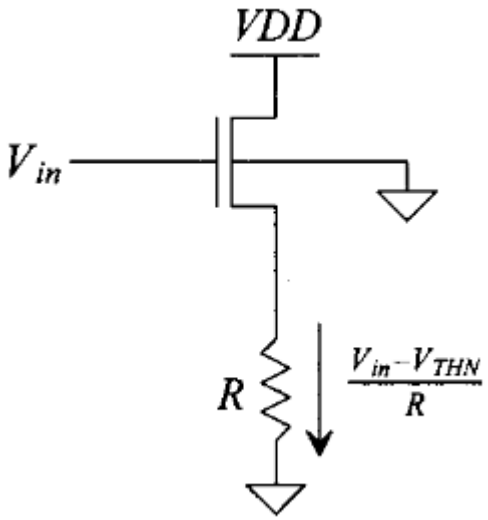
P14. For the following voltage to current converter, the resistor value is given as 10 MΩ and VDD =5V is applied. For an input voltage ranging from 1V to 5V:

a) Simulate the circuit

b) Show that the I_{out}-V_{in} simulated is not linear?

c) What is the ideal slope for the given circuit?

Use long-channel device.



P15. For an nMOS long channel transistor, simulate a circuit using LT spice that outputs the threshold voltage versus the source to body voltage.