Scaling Issues in Planar FET: Dual Gate FET and FinFETs

Lecture 12

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Outline

- Scaling Issues for Planar MOSFET:
  - Subthreshold Slope
  - Drain Induced Barrier Lowering (DIBL)
  - Threshold Voltage
  - Doping effect on:
    - Mobility
    - Junction Leakage due to Band-to-Band Tunneling
  - Junction Capacitance
- Silicon on Insulator (SOI)
- Dual Gate FET
- FinFET

Subthreshold Current and Slope for Planar "Long Channel" MOSFET

$$I_{ds\ subth} = \mu_{neff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{gs}-Vt)}{mkT}} \left[1 - e^{-qVds/kT}\right]$$

At $V_{gs} = 0$: $I_{ds\ Off}$=*Off-state leakage current* $\approx I_o e^{\frac{-qVt}{mkT}}$

-> *Ids leakage increase exponentially with decreasing V_t or increasing T*

$$S = \left(\frac{d\ log_{10}\ Ids}{dV_{gs}}\right)^{-1} = 2.3\left(\frac{m\ kT}{q}\right) = 2.3\left(\frac{kT}{q}\right)\left(1 + \frac{C_{dm}}{C_{ox}}\right) \approx 2.3\left(\frac{kT}{q}\right)\left(1 + \frac{3t_{ox}}{W_{dm}}\right)$$

Expressed in mV/decade

- As L decreases, V_t decreases, and both *S* and I_{subth} degrade
- One solution is to minimize the body effect coefficient *m* by decreasing C_{dm} w.r.t. C_{ox}:
  - Double C_{ox} for a given C_{dm}
  - Increasing W_{dm} worsens SCE

Drain-Induced Barrier Lowering and ΔVt

- From psuedo-2D Analysis the lowering of V_t is:

$$\Delta V_t = 8(m-1)[\sqrt{\Psi(V_{bi}+Vds)} - \frac{11\,t_{ox}}{W_{dm}}]\, e^{-\pi L/[2(W_{dm}+3t_{ox})]}$$

$$V_t = V_{to} - \Delta V_t$$

The lowering of ΔV_t increases exponentially with increasing the ratio of $(W_{dm}+3t_{ox}) = mW_{dm}$ w.r.t. L

- Try to minimize both W_{dm} and t_{ox}
- $m = 1 + 3t_{ox}/W_{dm}$ increases with a smaller W_{dm}, but at slower rate because of the "1" term, and because of scaling down of t_{ox}
- Decreasing ΔV_t exponentially by decreasing $(W_{dm}+3t_{ox})$ decreases in turn I_{off} and S
- Keep L ~2-3 times W_{dm}

Psuedo-2D Analysis of Short Channel Subthreshold Slope

$$S \approx 2.3\frac{mKT}{q}\left(1+\frac{11\,t_{ox}}{W_{dm}}e^{-\pi L/[2(W_{dm}+3t_{ox})]}\right)$$
$$= S_o\left(1+\frac{11\,t_{ox}}{W_{dm}}e^{-\pi L/[2(W_{dm}+3t_{ox})]}\right)$$

Where S_o is the long channel value of S

Again:

- Minimize both W_{dm} and t_{ox}
- Keep L ~2-3 times W_{dm}

S/D Diode Junction Leakage and Capacitance

- S/D reverse current from bottom of S/D junctions and sidewalls of junction
- Band-to-band tunneling
- S/D *pn* junction depletion capacitance depends as well on area (bottom area + sidewall area)
  - Additional capacitance means higher parasitics and slower FET

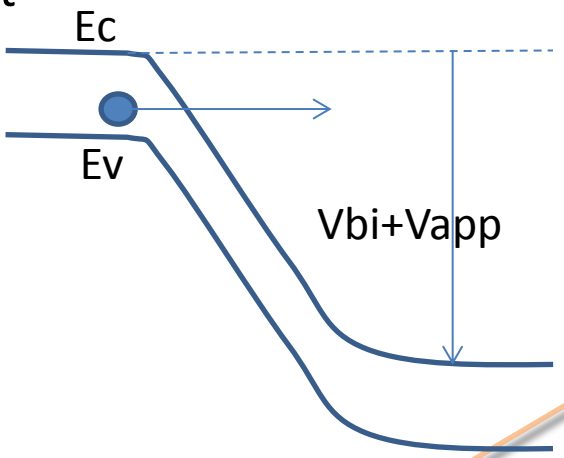
S/D Band-to-Band Tunneling

$$J_{B-B} = K_o E\, V_{app} \exp\left(-\frac{E_0}{\mathrm{E}}\right)$$

Where

$$Electric\ Field = E = \sqrt{\frac{2qN_A(V_{app} + V_{bi})}{\epsilon_{si}}}$$

- J_{BB} increases exponentially with $\sqrt{N_A}$, in addition to the pre-factor
- Increasing N_A to suppress short channel effects (SCE) exponentially increases S/D *pn* junction leakage current



S/D Depletion Capacitance Dependence on Doping

$$C_{diode\ dep} = \sqrt{\frac{\epsilon_{si} q N_A}{2(V_{bi}+V_{ds})}}$$

- Increasing N_A to suppress short channel effects (SCE) increases S/D *pn* junction depletion capacitance as a factor of $\sqrt{N_A}$

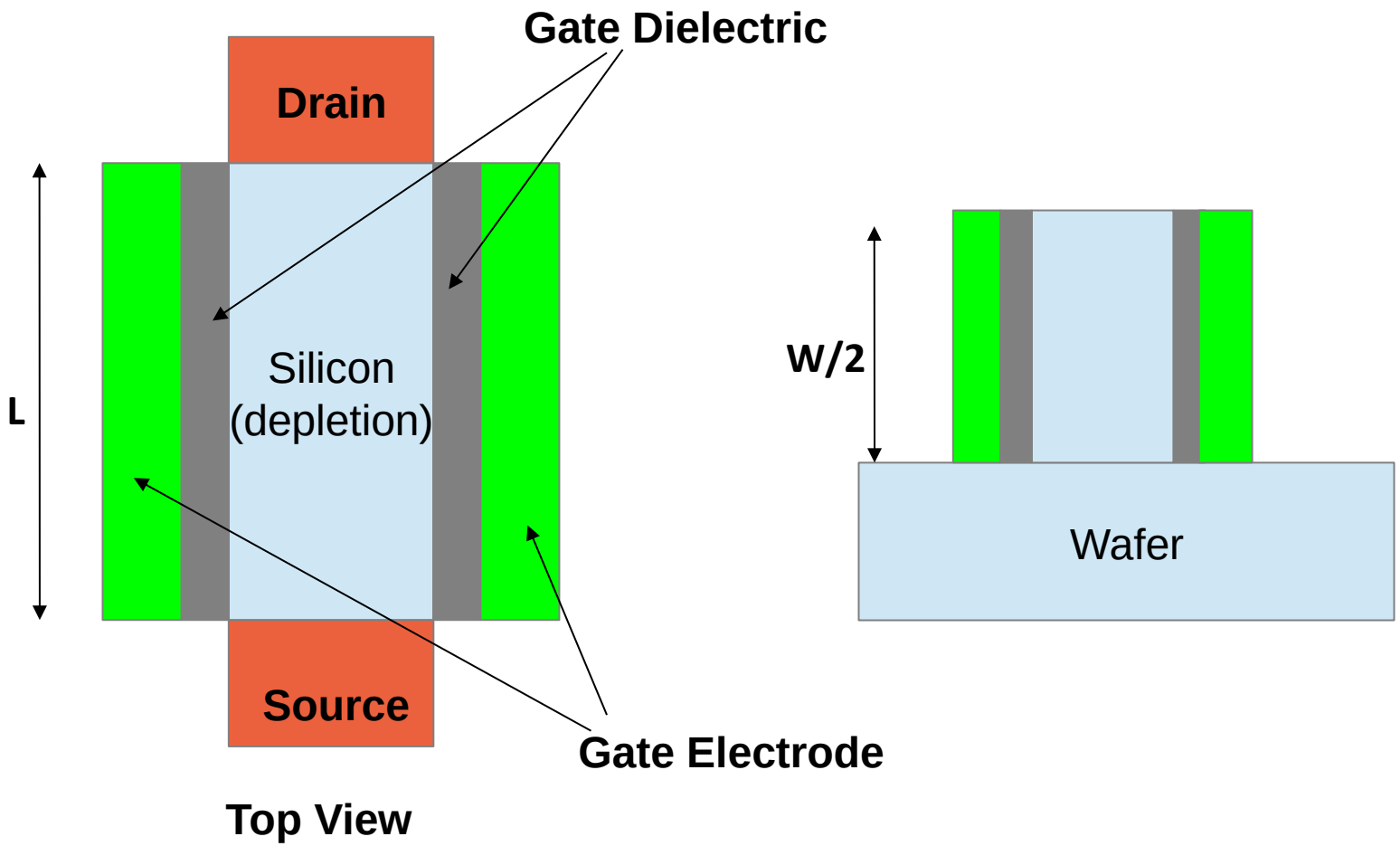
Fully Depleted Silicon-on-Insulator (FD-SOI)

- Solves one of the problems: limit W_{dm} w.r.t. L
- Solves the junction leakage and capacitance

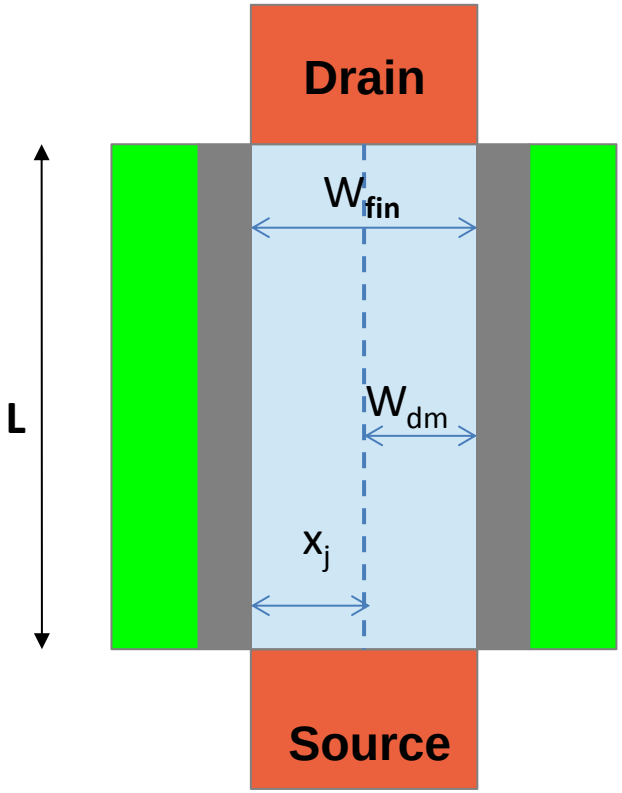
FinFET: Dual Gate

- Doubles the control of the gate over the depletion region
- Double the channel Width using same footprint: higher W/L
- Controlled depletion width, independent from doping
- Allows near-intrinsic doping: higher mobility

Dual Gate FinFET



New W_{dm} and xj



Top View

$$W_{dm} = \frac{H_{fin}}{2}$$

$$x_j = \frac{H_{fin}}{2}$$

Solution of S/D Leakage and Capacitance by Dual Gate FET

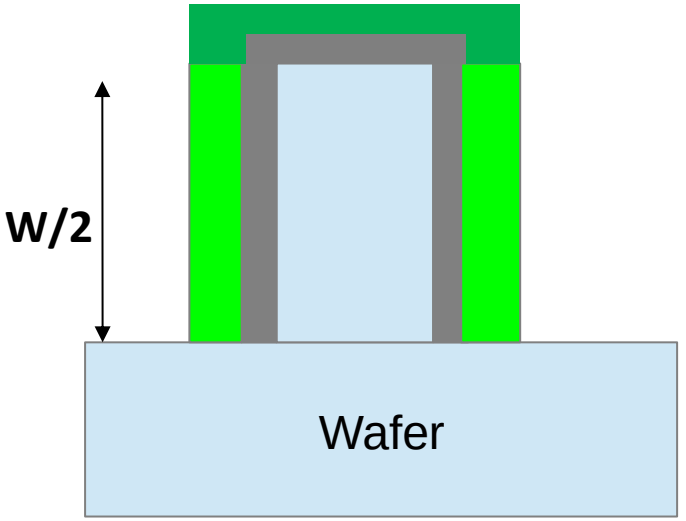
- The leakage current from the bottom area of the S/D have been totally eliminated
- Only one sidewall contributes to leakage in each junction
- Possible reduction in substrate doping to near 10^{15}cm, since W_{dm} is not controlled by N_A any more
  - Reduction in Band-to-Band tunneling current for S/D

Doping Effect on Mobility

- Effective mobility (both for bulk and surface) decreases with increasing substrate doping NA
- Increasing N_A to suppress short channel effects (SCE) decreases mobility
- Surface mobility also degrades more due to increased effective field by increasing NA
- For Dual Gate FET:
  - Possible reduction in substrate doping to near 10^{15}cm, since W_{dm} is not controlled by N_A any more
  - This increases mobility and current

Triple Gate: FinFET

- Gate and dielectric on top as well



Metal Gate / High-k Dielectrics

Metal Gates

- Eliminates polysilicon gate depletion: smaller electrical t_{oxe}
- Improves the gate resistance, especially RC distributed effect

High-k Dielectrics

- Thicker physical thickness can be used to achieve an equivalent thinner oxide thickness since it has higher dielectric constant:
  - Less gate leakage
  - Standardized on HfO_2 wit $\epsilon_r \approx 25 \rightarrow t_{dielectric} = \frac{25}{3.9} t_{oxide}$
- Achieves total equivalent oxide $t_{ox} < 1nm$
- Typically a thin (0.5nm) SiO_2 interface layer (IL) with silicon