COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications Engineering

Instructor: Dr. Amr Bayoumi

Course Title: Modern Electronics Circuits

Course No.: EC560 Assignment 3

Date: March 5, 2016

Bandwidth and High Speed Amplifiers

Note: For **all transistors:**

- Use the 2nd Edition of the textbook
- Use -N-MOSFETs with the BSIM model in page 190
- Use W = 100um, Lgate = 0.5um, Source and drain dimensions are W x 2um
- Assume that in short channel, Ids = Idso(1 + Vds/VA), VA=10V, where Idso is current at velocity saturation, assuming no short channel effects on Vto or Leff.
- Use velocity saturation and channel length modulation for short channel at high Vds
- Assume Vgs=Vgs=3.3V for all problems. You shouldstart by finding, gm, gd, Cgs, Cgd. Ignore Csb, but keep Csd. Ignore RE

Question 1 :

Derive equation 13 p. 152.

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Question 2 :

Using QUCS to simulate circuits for Fig. 7.2 and 7.6, and compare the BW of each. Use the transistor technology file of 0.5um from p. 190.

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Question 3 :

For the circuit in Fig. 8.1, design a shunt peak load for the transistor, using m which gets a flat response. Calculate the BW before and after. Assume the original circuit had an RL = 200Ohm, CL = 2pF

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Question 4 :

Use a zero-peaked configuration to improve the bandwidth of Fig. 8.1, again with RL = 200Ohm, CL = 2pF.

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Question 5 :

Design a tuned amplifier with fo = 100MHz, BW=10MHz. Assume CL= 1pF, Rs=1KOhm.

Take MOS parasitics in output into effect, as needed. Take eqn. 39 p. 202 into account.

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Question 6 :

Use circuit in Fig. 8.20, p205, to improve the miller capacitance in previous question. Redesign the circuit to meet requirements if Q5.

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Question 6 :

Assume we have 3 circuits as the one in Fig. 8.1, connected in series as a cascade configuration. Find the overall BW. Assume each stage has an RL= 200 Ohm, CL = 2pF, and zero Rs.