Simplified Generic On-line PWM Technique for Single Phase Grid Connected Current Source Inverters

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***Abstract*— Mandatory restrictions for a current source inverter's (CSI's) proper operation, like continuity of the DC link current, complicate the corresponding PWM generation especially in the case of single phase systems. Classical modulation techniques for single phase CSIs suffer from either complexity or unsymmetrical gate signals distribution for the inverter switches. In this paper, a PWM generation technique suitable for single phase CSI's is presented. The proposed technique ensures CSI's adequate operation with the advantages of: (i) Simple generic on-line implementation, (ii) Better utilization of the carrier frequency and (iii) Symmetrical distribution of the inverter's gate signals that ensures equal loss sharing, conduction and switching, among the inverter power semiconductors. System results, using simulations in addition to experimental setup, are utilized to validate the effectiveness of the proposed technique.**

I. INTRODUCTION

Current source inverters (CSI's) are highly competitive to voltage source inverters. The ability of near sinusoidal voltage generation, inherent short-circuit proof and regeneration capabilities of the CSI's create their promising penetration in the converters' market [1].

The development in CSI's topologies witnessed less attention than their modulation techniques. Early stages of CSI's utilization depend on the famous simply implemented quasi-square wave modulation with the penalty of highly distorted waveforms [2-5]. Traditional implementation in medium voltage drives limits the carrier frequency in CSI's modulation, hence selective harmonics elimination (SHE) PWM technique is widely used in these applications with the drawback of generally being offline [6-11] even with hybrid SHE- trapezoidal modulation [12-13]. Dynamic bilogic to trilogic translation enhances linear current feedback control algorithms but with complex computational load due to the need of decoupler processing stage and programmable array logic (PAL) translator [14-15]. As CSI's modulation is tied up with mandatory restriction, the DC link path must not be interrupted, efficient sophisticated carrier-based PWM techniques suitable for VSI's are difficult to implement. Therefore, the addition of extra power semiconductors to the conventional CSI topology, to ensure the continuity of the DC link current, was the primary solution [16-18] creating cost and hardware complexity drawbacks.

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The innovative duality theory between VSIs and CSIs enables state mapping, thus conventional PWM techniques for VSIs can be mapped to suit conventional CSI's topologies without neither being offline nor the need to add extra semiconductors [19-21]. The state mapping enhance the control capabilities of CSI's to reach higher and faster performance like bang-bang based voltage control strategies [22-23]. As an important extent and achievement for the duality theory, the on-line generation of CSI PWM pulses from those of conventional VSI was remarked as the clue for generating on-line continuous variable-modulation-index PWM techniques for conventional topology CSI's using traditional VSI's PWM generators [24-28].

Despite of the intensive research related to CSI's PWM techniques presented in literature [2-28], the majority of such techniques were dedicated to three-phase CSI's. Limited attention was given to single phase CSI's although they are promising power conversion systems for modern distributed generation. Noticeable attempt to overcome the restriction of the DC link current continuity in single phase CSI's by operating as a soft-switching converter with additional semiconductors to secure the DC current path [29] again with the same drawback of extra hardware similar to the three-phase CSI [14-16].

The most common technique for single phase CSI's originally represented in late 90's [30] and recently enhanced [31-34] relies on sinusoidal pulse width modulation (SPWM) base. The DC link current restriction is solved by maintaining the upper switches ON for half the fundamental cycle and the lower switches are sinusoidally modulated. Although simple and efficient, this technique suffers from several drawbacks mainly the unsymmetrical utilization of the upper and lower semiconductors, unequal losses distribution and low carrier frequency utilization.

In this paper, a simplified on-line PWM generation technique for single phase CSI's is presented. The proposed technique is a modified version of the three-phase on-line generation technique based on the duality theory [24-28]. In addition to fulfill CSI's general gating condition restrictions, several advantages are gained.

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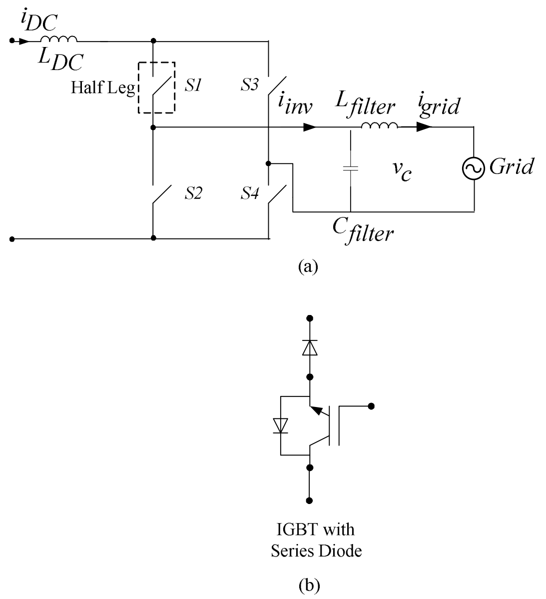


Fig. 1: Single phase grid connected CSI: (a) Topology, (b) Half-leg configuration

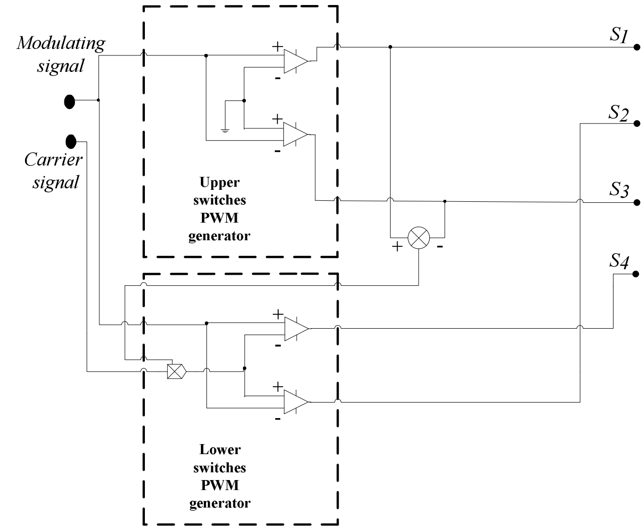


Fig. 2: Classical single phase CSI PWM generation

The presented technique achieves simple implementation, generic on-line capability, equal distribution of the shoot-through pulses and uniform losses distribution among the inverter's semiconductor devices.

The presented paper is organized in six sections. Following the introduction, the single phase CSI's classical PWM technique is illustrated in the second section. The proposed on-line PWM generation technique is presented in the third section. Simulations and experimental results are addressed and discussed in sections four and five respectively. Finally, a conclusion is given in the sixth section.

II. SINGLE PHASE CSI'S CLASSICAL PWM MODULATION TECHNIQUE

In this section, brief introduction and analysis of classical PWM modulation suitable for single phase grid connected CSI [30-34] is presented. Fig. 1 shows the conventional topology of single phase CSI that includes DC choke, four semiconductor switches, CL line filter, and grid connection. The main principle of the classical PWM technique for single phase CSI is sinusoidal based modulation where a sinusoidal reference, with the fundamental frequency, is compared with a triangular carrier. The main issue is how to create the shoot-through pulses and distribute them. For simplicity, the two upper semiconductor switches (S1 and S3) are conducting for half the cycle while the two lower switches (S2 and S4) are modulated simultaneously. By this way, the DC link current path's continuity is ensured for the whole cycle. The block diagram of this technique is illustrated in Fig. 2 while Fig. 3 shows the CSI's pulse generation signals.

As shown in Fig. 2, the classical PWM generation circuit is simple as it utilizes only four comparators, one summing point and one multiplier. The circuit, although can be a mixed analog/digital hardware realization, is much easier to be software implemented. As shown in Fig. 3, the classical PWM technique creates unequal pulses distribution for the CSI.

Therefore, upper semiconductor switches suffers from higher conduction losses than the lower ones due to their longer conduction period while the contrary occurs from the switching losses point of view as only the lower semiconductors are being modulated.

III. PROPOSED SINGLE PHASE CSI'S PWM MODULATION TECHNIQUE

The proposed on-line modulation technique for single phase CSI's is illustrated in this section. Fig. 4 shows the proposed technique realization. As it can be noticed, the proposed PWM generation technique consists mainly of four blocks:

A. *Conventional SPWM VSI switching generator*

This block utilizes the modulating and the carrier signals to generate PWM pulses suitable for VSI (g1-g4). This block is a classical PWM generator that can be easily built as hardware or software implemented by any C-compiler available today in most of the off-the-shelf market available micro-controllers. These pulses (g1-g4) are not suitable yet to gate a CSI.

B. *Complementary pulse generator*

This stage creates a shoot-through signal (SHT) that is active when an open circuit occurs due to an off-state either due to the upper switches (g1, g3) or the lower switches (g2, g4) from the VSI pulses (g1-g4).

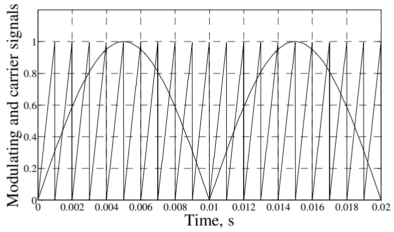
Basically, this stage gives pulses that correspond to the open circuit states in VSI PWM that needs to be mapped to short circuit states in CSI gating. Therefore this stage's name comes from this point.

C. *Complementary pulse distributer*

The role of this stage is to distribute the short circuit states (shoot-through pulses, SHT) between the CSI's legs to create equal stress distribution on the inverter power semiconductors. Two signals output from this stage (x1, x2). The first signal (x1) is a square wave for the positive half cycle of the modulating signal while in the negative period it is zero. The second signal (x2) is the complement of the first one (x1).

D. Pulse combinator

In this stage, two signals (d1, d2) are generated from the complementary pulse signal (SHT) and the complementary pulse distributer output signals (x1, x2). The signals (d1, d2) are the equally distributed shoot-through pulses for the positive and negative half cycles. The VSI gate signals (g1-g4) are updated by (d1, d2) to generate PWM signals suitable for CSI with uniform equally distributed short circuit states (S1-S4).



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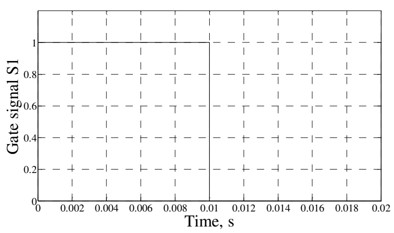

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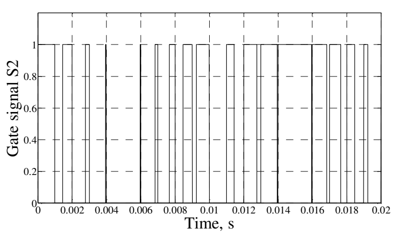

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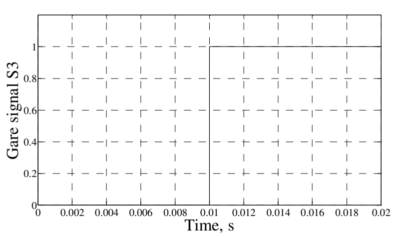

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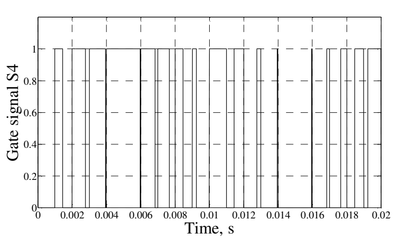

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Fig. 3: Single phase CSI's classical PWM technique for one cycle simulation, unity modulation, 1 kHz switching
(a) Modulating and carrier signals, (b-e) S1-S4 gating signals in p.u

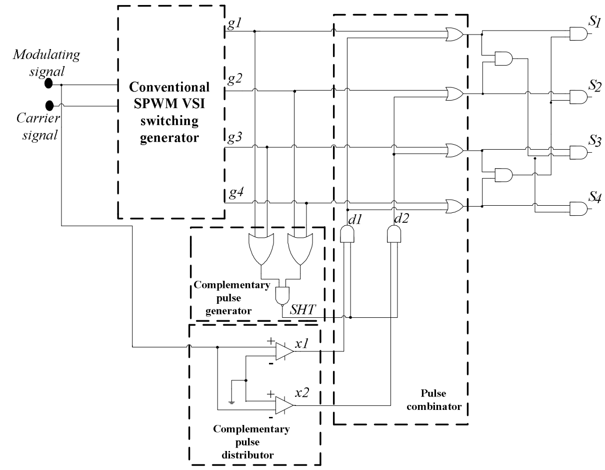
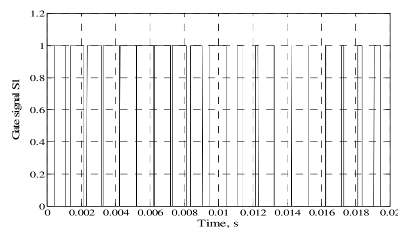


Fig. 4: Proposed single phase CSI PWM generation technique



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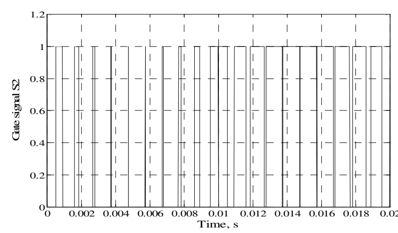

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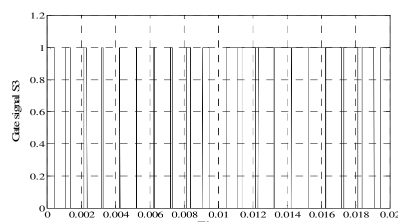

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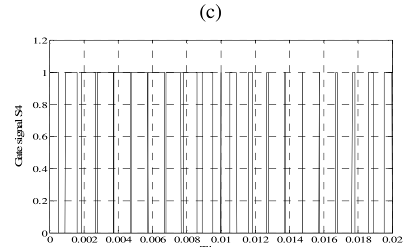

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Fig. 5: Single phase CSI's proposed PWM technique for one cycle simulation, unity modulation, 1 kHz switching
(a-d) S1-S4 gating signals in p.u

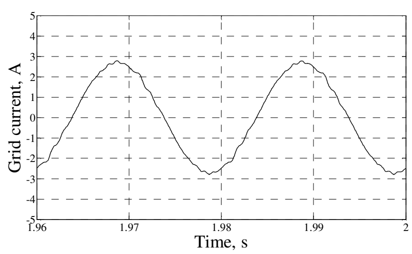
IV. SIMULATION RESULTS

For proper illustration of the proposed modulation technique advantages, a comparison between the classical and the proposed techniques is held using simulation results. The system under simulation is a single phase grid connected CSI. The grid voltage is assumed to be ripple-free and of peak voltage 311V at 50Hz. The DC link current is simulated to be ripple-free in order to focus on the effect of the modulation implementation solely on the grid current distortion.

As a single phase system, conventional Proportional Integral (PI) controllers are not suitable hence Proportional Resonant (PR) controller is utilized instead as a grid current controller. The comparison is held from three points of view: grid current, inverter current, and capacitor voltage. For fare comparison, both systems are compared with the same switching frequency (1 KHz) and same AC line filter components (filter capacitance is 25μF and filter inductance is 10mH).

A. Grid current

The grid current for both the classical and the proposed modulation technique are illustrated in Fig. 6. As shown in Fig. 6, the grid current in the case of the proposed modulation technique is better, from harmonics point of view, than that generated using the classical modulation technique when using the same carrier frequency and line filters.



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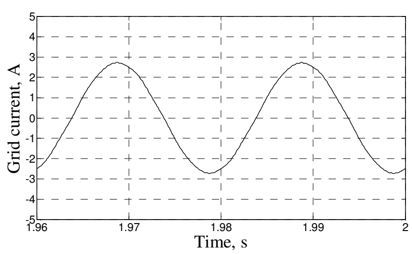

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Fig. 6: Grid current, one cycle simulation
(a) Classical, (b) Proposed

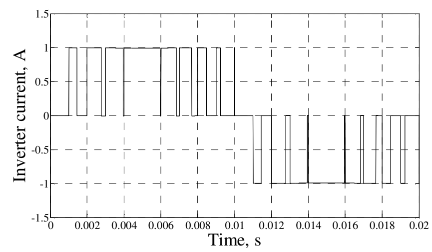
B. Inverter current

In this section, the inverter current is illustrated and compared between the proposed and classical technique as shown in Fig. 7.

Fig. 7 shows that with the proposed technique, the inverter current is constructed from higher number of pulses than when using the classical technique with the same carrier frequency. This is mainly due the drawback of the classical technique in asymmetrically modulating the inverter switches. On the contrary, the proposed technique offers equal symmetrical gating for the inverter switches, hence higher number of pulses for the same carrier frequency is achieved.

C. Inverter voltage

This subsection is mainly concerned with the capacitor voltage quality. Although, the capacitor voltage quality is of less importance than the grid current for grid connected applications, it is vital for off-grid/stand-alone applications like uninterruptable power supplies, distributed generation power converters, and voltage sag correctors. The capacitor voltage with the grid voltage is illustrated in Fig. 8 for the classical and the proposed modulation techniques. As can be interpreted from the previous subsections, the quality of the inverter is enhanced due to the proposed modulation technique.



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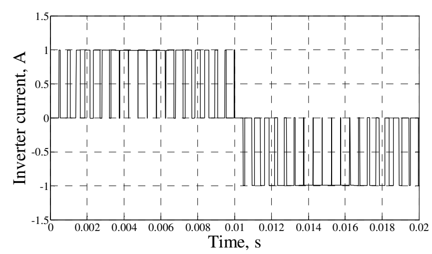

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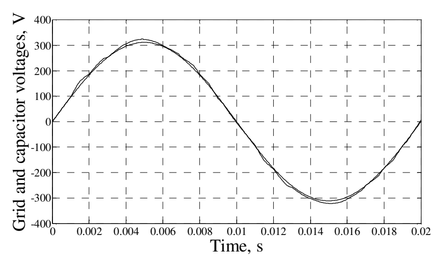
Fig. 7: Inverter current, one cycle simulation
(a) Classical, (b) Proposed



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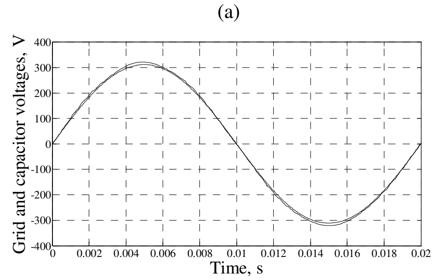

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Fig. 8: Capacitor and grid voltages, one cycle simulation
(a) Classical, (b) Proposed

V. EXPERIMENTAL RESULTS

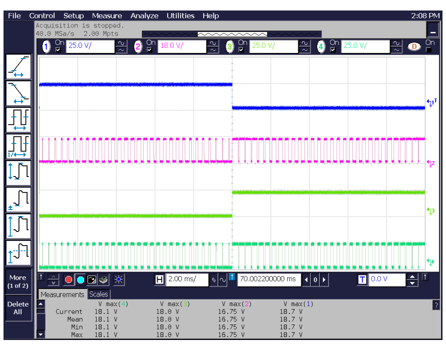
For more illustration of the proposed technique and emphasis on its validity, an experimental rig is prepared. The prepared experimental setup is a single phase grid connected system with grid current control using PR controllers and 3 kHz switching frequency. Table. I lists the experimental setup elements.

Table. I
Experimental setup elements' list

Element	*Value/Manufacturer*
Target board DSP	TI TMS320F28335
Inverter IGBT (4)	FGL60N100BNTD
Inverter series fast diode (4)	IXYS DSEI60-10A
Voltage transducer	LEM LV20-P
Current transducer	LEM HAS50-S
Gate drivers	Semikron SKHI22AH4R
DC link inductor	50 mH
Filtering capacitor	25 μF
Filtering inductor	10 mH

The experimental results are shown in Figs. 9 - 11. As shown in Fig. 9, the proposed technique offers uniform symmetrical distribution of the inverter gating signals, thus providing equal losses distribution of the utilized semiconductors.

Another advantage of the proposed technique is the better utilization of the carrier frequency. As shown in Fig. 10, the inverter current in the proposed technique case offer higher number of pulses than the classical technique for the same carrier frequency. Consequently, this is reflected on the grid current and capacitor voltage quality as shown in Fig. 11.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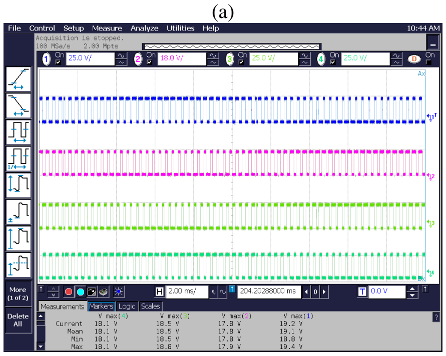
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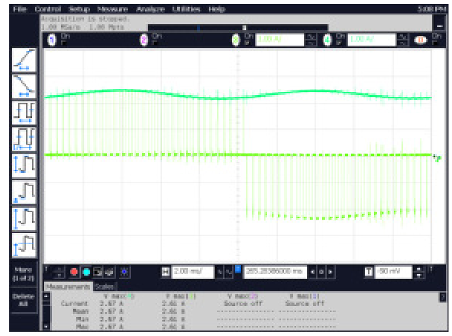
Fig. 9: Gating signals experimental results
(a) Classical, (b) Proposed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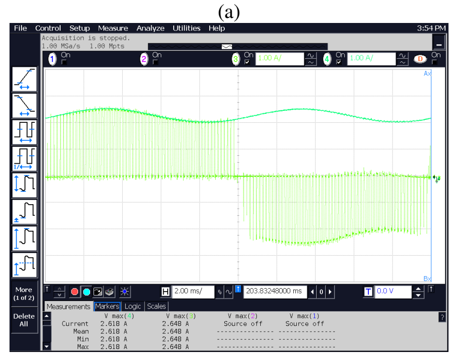
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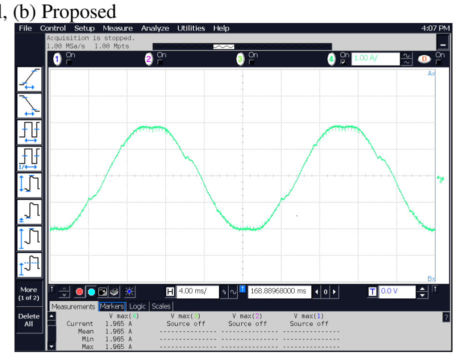
Fig. 10: Inverter and DC link currents experimental results
(a) Classical, (b) Proposed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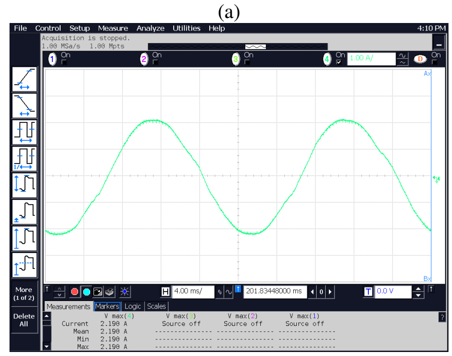
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Fig. 11: Grid current experimental results
(a) Classical, (b) Proposed

VI. CONCLUSION

In this paper, a single phase CSI's PWM modulation technique has been presented. Classical modulation technique has been illustrated with emphasis on its major drawbacks like unsymmetrical distribution of the inverter gating signals.

Advantages of the proposed technique have been illustrated. Among them, equal gating signals distribution, better utilization of the carrier frequency and simple on-line implementation. In addition to simulations, an experimental setup is carried out that shows the proposed technique effectiveness.

ACKNOWLEDGMENT

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REFERENCES

[1] Wu, B.: 'High Power Converter Systems' (IEEE Press and John Wiley, 2006).

[2] Kim, Gi Taek; Chun, Tae Won; Sul, Seung Ki; Park, Min Ho; , "Design of Single-Chip Microprocessor-Based Controller for Current Source Inverter-Fed Induction Motor Drive," Industrial Electronics, IEEE Transactions on , vol.IE-34, no.3, pp.331-338, Aug. 1987

[3] Biswas, Sujit K.; Basak, B.; Sathiakumar, S.; Vithayathil, Joseph; , "A New Three-Phase Current Source Inverter with Flexible PWM Capability," Industry Applications, IEEE Transactions on , vol.IA-23, no.5, pp.921-926, Sept. 1987

[4] Bowes, S.R.; Bullough, R.I.; , "Novel PWM controlled series-connected current-source inverter drive ," Electric Power Applications, IEE Proceedings B , vol.136, no.2, pp.69-82, Mar 1989

[5] Trzynadlowski, A.M.; Patriciu, N.; Blaabjerg, F.; Pedersen, J.K.; , "A hybrid, current-source/voltage-source power inverter circuit," Power Electronics, IEEE Transactions on , vol.16, no.6, pp.866-871, Nov 2001

[6] Matsuse, K.; Kubota, H.; , "Analysis of PWM current source GTO inverter with PWM-controlled thyristor rectifier for induction motor drive," Industry Applications, IEEE Transactions on , vol.26, no.2, pp.274-282, Mar/Apr 1990

[7] Enjeti, P.N.; Ziogas, P.D.; Lindsay, J.F.; , "A current source PWM inverter with instantaneous current control capability," Industry Applications, IEEE Transactions on , vol.27, no.3, pp.582-588, May/Jun 1991

[8] Matsuse, K.; Kubota, H.; Huang, L.; , "Performance of PWM-controlled thyristor rectifier operating at unity fundamental power factor in PWM current source GTO inverter system for induction motor drives," Industry Applications, IEEE Transactions on , vol.30, no.3, pp.699-706, May/Jun 1994

[9] Karshenas, H.R.; Kojori, H.A.; Dewan, S.B.; , "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters," Power Electronics, IEEE Transactions on , vol.10, no.5, pp.566-573, Sep 1995

[10] Yuan Xiao; Bin Wu; DeWinter, F.A.; Sotudeh, R.; , "A dual GTO current-source converter topology with sinusoidal inputs for high-power applications," Industry Applications, IEEE Transactions on , vol.34, no.4, pp.878-884, Jul/Aug 1998

[11] Zargari, N.R.; Rizzo, S.C.; Xiao, Y.; Iwamoto, H.; Satoh, K.; Donlon, J.F.; , "A new current-source converter using a symmetric gate-commutated thyristor (SGCT)," Industry Applications, IEEE Transactions on , vol.37, no.3, pp.896-903, May/Jun 2001

[12] Wu, B.; Slemon, G.R.; Dewan, S.B.; , "PWM-CSI induction motor drive with phase angle control," Industry Applications, IEEE Transactions on , vol.27, no.5, pp.970-976, Sep/Oct 1991

[13] Bin Wu; Dewan, S.B.; Slemon, G.R.; , "PWM-CSI inverter for induction motor drives," Industry Applications, IEEE Transactions on , vol.28, no.1, pp.64-71, Jan/Feb 1992

[14] Wang, X.; Ooi, B.-T.; , "Unity PF current-source rectifier based on dynamic trilogic PWM," Power Electronics, IEEE Transactions on , vol.8, no.3, pp.288-294, Jul 1993

[15] Kazerani, M.; Zhong-Chao Zhang; Boon-Teck Ooi; , "Linearly controllable boost voltages from Tri-Level PWM current-source inverter," Industrial Electronics, IEEE Transactions on , vol.42, no.1, pp.72-77, Feb 1995

[16] Joos, G.; Moschopoulos, G.; Ziogas, P.D.; , "A high performance current source inverter," Power Electronics, IEEE Transactions on , vol.8, no.4, pp.571-579, Oct 1993

[17] Moschopoulos, G.; Joos, G.; Ziogas, P.D.; , "Input characteristics of variable modulation index controlled current source inverters," Industrial Electronics, IEEE Transactions on , vol.41, no.2, pp. 216-223, Apr 1994

[18] Nonaka, S.; Neba, Y.; , "Current regulated PWM-CSI induction motor drive system without a speed sensor," Industry Applications, IEEE Transactions on , vol.30, no.1, pp.116-125, Jan/Feb 1994

[19] Ledwich, G.; , "Current source inverter modulation," Power Electronics, IEEE Transactions on , vol.6, no.4, pp.618-623, Oct 1991

[20] Holmes, D.G.; , "A unified modulation algorithm for voltage and current source inverters based on AC-AC matrix converter theory," Industry Applications, IEEE Transactions on , vol.28, no.1, pp.31-40, Jan/Feb 1992

[21] Zmood, D.N.; Holmes, D.G.; , "Improved voltage regulation for current-source inverters," Industry Applications, IEEE Transactions on , vol.37, no.4, pp.1028-1036, Jul/Aug 2001

[22] Colli, V.D.; Cancelliere, P.; Marignetti, F.; Di Stefano, R.; , "Influence of voltage and current source inverters on low-power induction motors," Electric Power Applications, IEE Proceedings - , vol.152, no.5, pp. 1311- 1320, 9 Sept. 2005

[23] Colli, V.D.; Cancelliere, P.; Marignetti, F.; Di Stefano, R.; , "Voltage control of current source inverters," Energy Conversion, IEEE Transactions on , vol.21, no.2, pp. 451- 458, June 2006

[24] J. Espinoza; G. Joos; , "On-line generation of gating signals for current source converter topologies," Industrial Electronics, 1993. Conference Proceedings, ISIE'93 - Budapest., IEEE International Symposium on , vol., no., pp.674-678, 1993

[25] Espinoza, J.R.; Joos, G.; , "Current-source converter on-line pattern generator switching frequency minimization," Industrial Electronics, IEEE Transactions on , vol.44, no.2, pp.198-206, Apr 1997

[26] Graovac, D.; Katic, V.; , "Online control of current-source-type active rectifier using transfer function approach," Industrial Electronics, IEEE Transactions on , vol.48, no.3, pp.526-535, Jun 2001

[27] Loh, P. C.; Vilathgamuwa, D. M.; Gajanayake, C. J.; Wong, L. T.; Ang, C. P.; , "Z-Source Current-Type Inverters: Digital Modulation and Logic Implementation," Power Electronics, IEEE Transactions on , vol.22, no.1, pp.169-177, Jan. 2007

[28] Suh, Y.; Steinke, J.K.; Steimer, P.K.; , "Efficiency Comparison of Voltage-Source and Current-Source Drive Systems for Medium-Voltage Applications," Industrial Electronics, IEEE Transactions on , vol.54, no.5, pp.2521-2531, Oct. 2007

[29] Itoh, R.; Ishizaka, K.; Oishi, H.; Okada, H.; , "Soft-switched current-source inverter for single-phase utility interfaces," Electronics Letters , vol.37, no.20, pp.1208-1209, 27 Sep 2001

[30] Hirachi, K.; Tomokuni, Y.; , "A novel control strategy on single-phase PWM current source inverter incorporating pulse area modulation," Power Conversion Conference - Nagaoka 1997., Proceedings of the , vol.1, no., pp.289-294 vol.1, 3-6 Aug 1997

[31] Neba, Y.; , "A simple method for suppression of resonance oscillation in PWM current source converter," Power Electronics, IEEE Transactions on , vol.20, no.1, pp. 132- 139, Jan. 2005

[32] Li, R.T.H.; Henry Shu-hung Chung; Chan, T.K.M.; , "An Active Modulation Technique for Single phase grid Connected CSI," Power Electronics, IEEE Transactions on , vol.22, no.4, pp.1373-1382, July 2007

[33] Komurcugil, H.; , "Steady-State Analysis and Passivity-Based Control of Single-Phase PWM Current-Source Inverters," Industrial Electronics, IEEE Transactions on , vol.57, no.3, pp.1026-1030, March 2010

[34] Li, R.T.H.; Chung, H.S.-H.; Wing-Hong Lau; Zhou, B.; , "Use of Hybrid PWM and Passive Resonant Snubber for a Grid-Connected CSI," Power Electronics, IEEE Transactions on , vol.25, no.2, pp.298-309, Feb. 2010