Performance evaluation of optical logic gates using FWM

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In this study, we introduce a design of all-optical module for half-adder/half-subtracter and 2-to-4 decoder that generates simultaneously five of all-optical logic gates at 10 Gbps. These logic gates use dispersion compensation fiber (DCF) based on four-wave mixing (FWM). This design is integrated and economic. The various outputs can be manipulated by controlling nonlinear polarization rotation (NPR) which achieves low power requirements. The high performance confirms the effectiveness of all presented functionalities at optimized input data signals of 0.01 mW at 10^{-12} BER with an extinction ratio (ER) greater than 20 dB.

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1. Introduction

Future optical networks require ultrafast operations that are able to reduce the latency at nodes as well as to increase the available bandwidth, without affecting the traffic performance [1].

Optical signal processing overcomes the electronic bandwidth limitations with advantages in terms of transparency and scalability. In addition, similar to electric systems, even a few simple logic operations at a very high speed can dramatically improve system efficiency [1], and will play an important role in future optical fiber communication systems. Optical logic gates are key building blocks in many areas of optical signal processing. For example, the XOR logic gate is a commonly used device in half-adders/half-subtracters, pattern recognition circuits, ultrahigh-speed pattern generation, data encoding, and encryption circuits [2]. A lot of all-optical half-adder, full-adder, decoder, arithmetic units, and algebraic units are already proposed by several group of workers in the area of optical parallel computation [3]. The nonlinearities of optical fiber provide attractive functionalities for optical signal processing, such as four-wave mixing (FWM) [4, 5], cross-phase modulation (CPM) [6], and self-phase modulation (SPM) [7, 8].

All-optical logic gates based on semiconductor optical amplifier (SOA) are the most typical schemes, while the performance of the SOA based logic gates is limited by operation bit rates and pattern effects. Whereas, the logic gates based on the fiber nonlinearities are considered prospective in the high-speed operation due to their sub-picosecond ultrafast response [9]. Previously, many schemes have been demonstrated to realize varies digital signal processing (AND, NAND, OR, XOR, NOR,

XNOR) in the optical domain [10-15]. In particular, all-optical half-adder [16-18], and half-subtracter [19, 20] have been proposed and verified. The former can be applied to optical packet checksum calculation and binary counters, and the later may see its application in encryption and decryption of secure network data dual-direction binary counter [20]. However, the schemes above can realize different optical logic gates with different working parameters.

A novel scheme to realize all-optical logic gates is proposed based on NPR by the Kerr-effect in a single 0.07 km highly nonlinear dispersion compensation fiber (HNL-DCF) [21]. Due to the Kerr-effect, two different input lightwaves at λ_A and λ_B induce the DCF, thereby rotating the polarization state of a third lightwave at λ_C. The polarization of the lightwave can be controlled by the power and relative polarization of the pump power. Therefore, multiple all-optical logic gates are realized. At the same time half-adder/half-subtracter and decoder can be realized in a single coil of DCF. Both the theoretical analysis and the simulation demonstration of 10 Gbps optical "AND", "NOR", "XOR", "$A\bar{\cdot}B$", "$A\cdot\bar{B}$", half-adder/subtracter and decoder are proposed with RZ data.

All previous literatures that deal with designing, testing, and evaluating different all-optical logic combinational circuits using nonlinearity effects will be used together with additional related literatures to establish a comparison with our work and the in Section 6.

2. Concept of our technique

A conceptual diagram of our all-optical gates generation technique is shown in Fig. 1.

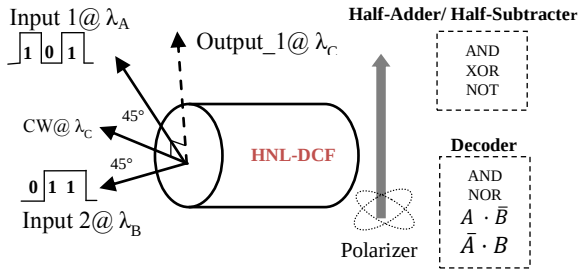

Fig. 1. Concept for all-optical gates based on single DCF

At the input of the HNL-DCF, the polarization states of the input waves at λ_A and λ_B are orthogonal to each other. Both of these inputs are aligned 45° with respect to the third continuous-wave (CW) signal at λ_C [2, 19, 22, 23]. A polarization is placed at the output of the HNL-DCF, aligned orthogonal to the original polarization state of λ_C. For "AND", "A $\bar{\cdot}$B", "A $\cdot\bar{B}$"and "XOR" when both λ_A and λ_B are OFF, there is no output at λ_C after the polarizer except universal gates as "NOR". When only the input signals at λ_A or λ_B are present, the Kerr-effect creates a difference in optical index between the polarization direction aligned with λ_A (for A $\cdot\bar{B}$) , λ_B (for A$\bar{\cdot}$B), or λ_C (for XOR) and the direction orthogonal to λ_B, λ_A or (λ_A and λ_B).

However, for "AND" when the input signals at λA and λB are present, there is an output at λ_C after the polarizer and no output for XOR or its parts. When only λ_A or λ_B are OFF or ON, the Kerr-effect creates a difference in optical index between the polarization direction aligned with λ_A or λ_B and the direction orthogonal to λ_C for XOR gate.

The phase difference results in the NPR in the fiber as expressed in Fig. 2. The polarization of the probe signal will change with and without the pump. Employing a polarizer with a proper polarization, with respect to the probe light, different all-optical logic gates can be realized.

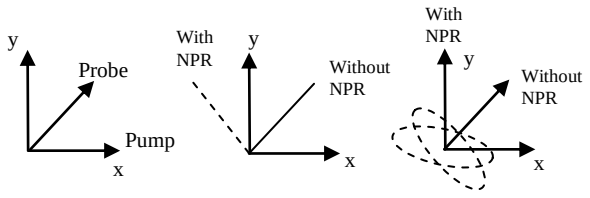

Fig. 2. Operation principle

By inducing a proper nonlinear phase shift in the HNL-DCF with adjusting the power and polarization of the lightwave as well as the polarization of the polarizer with respect to the polarization of lights, different optical logic gates can be achieved [19]. Considering that, the lightwave C is a linearly polarized continuous wave, which does not induce the nonlinear phase shift.

All optical half-adder (a combination of logic "XOR" and logic "AND"), and all optical half-subtracter (a combination of logic "XOR" and logic "A$\bar{\cdot}$B"or A$\cdot$B$\bar{}$), and all optical decoder (a combination circuit that converts binary information from n input lines to a maximum of 2n unique output lines) can be achieved, as all the necessary logic gates can be obtained at the same design and at the same time, as shown in Fig. 3.

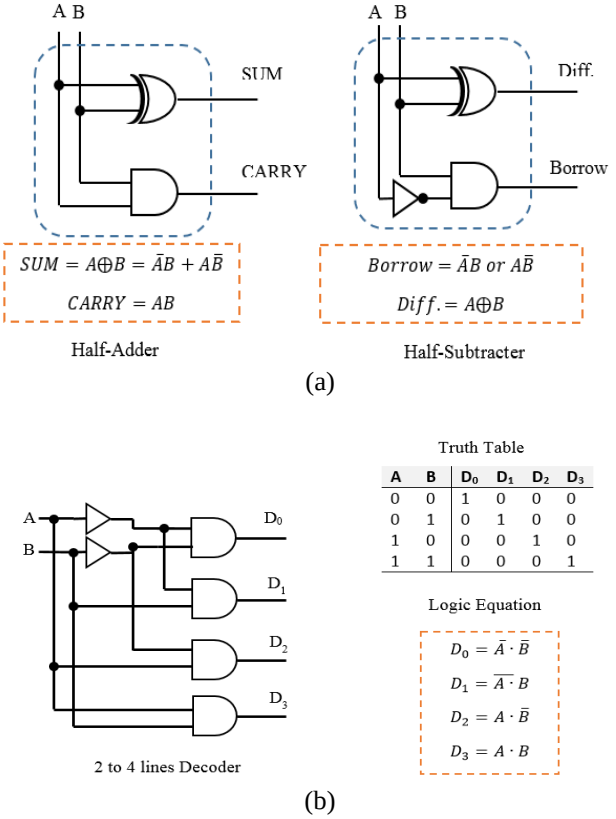

Fig. 3. Logic diagram of binary combinational logic circuits: (a) half-adder/half-subtracter; (b) 2-to-4 lines decoder

3. Simulation setup

We use Optisystem Software modeling tool to establish the simulation setup shown in Fig. 4. The components/parameters used to simulate the proposed system are extracted from related literature and famous vendors [2, 19, 24-28].Two independent data streams A and B at (λ_A = 1552.524 nm and λ_B = 1551.724 nm), with a peak power of the two input signals of 2.4 mW, with ER over 15 dB, together with the CW pump (λ_p = 1550.116 nm) are launched into the HNL-DCF waveguide. When the nonlinear interaction takes place under the NPR condition, this results in a phase difference at 10 Gbps bit rate, in which the FWM effect occurs. Optical return-to-zero (RZ) signals were generated by the CW laser array and two Lithium Niobate MachZehnder Modulator (LiNob3 MZM) in cascade, driven by a 10 Gbps data pattern with (2^{15}-1) pseudo random bit sequence (PRBS)

using pulse generator and 10 GHz sine wave, respectively. Tunable optical delay lines (ODL) were employed to decorrelate the optical signals A and B, and a polarization controller (PC) is used to control the relative polarization state between the two signals. Then, A, B and C are synchronized and combined together again by a wavelength division multiplexer/demultiplexer (WDM).

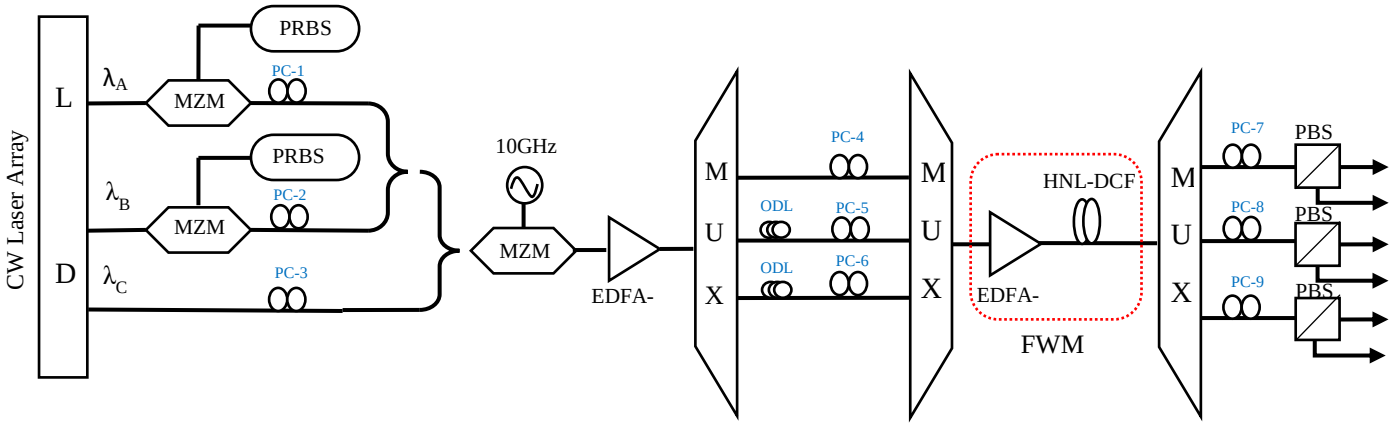

Fig. 4. Simulation setup (CW laser array, $LiNob_3$ MZM, EDFA, PC, WDM, DCF, OBPF and PBS)

4. Results and discussion

Table 1 summarizes the filtering wavelength, nonlinear phase shift and the relative polarization of the optical logic gates based on NPR in the HNL-DCF. BER and Q-factor analyzers are used to measure the downstream system performance.

Table 1. Functionality table of all-optical combination circuits

	$A \cdot B$	$A \cdot \bar{B}$	$\bar{A} \cdot B$	$\bar{A} \cdot \bar{B}$	$A \oplus B$
Filtering λ	λ_C	λ_A	λ_B	λ_c	λ_C
$\Delta\phi_N$	*orthogonal*			π	*orthogon*
φ	$\pi/4$	$\pi/4$	$\pi/4$	$\pi/2$	π
Half-Adder	CARRY				SUM
Half-Subtracter		Borrow			Diff.
Decoder	D_3	D_2	D_1	D_0	

It can be observed from Table 1 that, "A¯·B", "A ·B¯", "A·B", and "A⊕B\"", optical logic gates require the same nonlinear phase shift Δϕ_N where A and B, orthogonal to each other, means that the power requirement of lightwaves A, B, and C are the same. However, A and B are out of phase only for getting "A¯·B¯" , where the proper Later, the signals are amplified by using erbium doped fiber amplifier (EDFA) and are injected into a fiber of 0.07 km long HNL-DCF. The DCF has a nonlinear coefficient of 1.375 $W^{-1}km^{-1}$, and a near zero dispersion wavelength at 1550 nm. At the output of the HNL-DCF, another WDM and polarization beam splitters (PBS) are used to filter out the signals. They are used to choose the proper polarization of the signals in order to realize multiple logic gates. PC7, PC8, and PC9 are used to adjust the polarization of the output signal with respect to that of the polarization beam splitter. The scheme for all-optical half-adder/half-subtracter and 2-to-4 decoder makes no matter to apply to the higher data rate.polarization of the signals can be controlled by polarization angle φ of the output signal with respect to that of the PBS.

The simulation results were recorded by an optical time domain visualizer (OTDV), using a lightwave A with a bit sequence of "1001000111101010" and a lightwave B with a bit sequence of "0100011110101101", the corresponding RZ-OOK input signals have 2.4 mW as shown in Fig. 5 (a, b) and Fig. 6 (a, b).

For (d) in both Fig. 5 and Fig. 6, by filtering out the wavelength λ_B, the Boolean logic operation "$\bar{A} \cdot B$" is obtained, and for Fig. 6 (e), "$A \cdot \bar{B}$" is achieved by filtering out the wavelength λ_A. At the wavelength of the probe signal λ_C, the optical logic gates "NOR" and "XOR" are realized, which can be seen in Fig. 5 and Fig. 6, respectively.

Note that the entire logic gate can be achieved at the same time except universal logic gates "NOR". By combination, using the outputs mentioned in Table 1 and Fig. 3, all-optical combination circuits can be realized.

Referring to our design, first applicable circuits are the logic diagram of all-optical logic half-adder/half-subtracter, shown in Fig. 3 (a). So, the output logic bit pattern is presented in Fig. 5 (a) and Fig. 5 (b) as inputs of all-optical design, where Fig. 5(c) output of AND gate as carry of half-adder, Fig. 5 (d) Boolean logic operation $\bar{A} \cdot B$ as borrow for (B-A) and Fig. 5 (e) output of XOR

gate explains two functions: SUM of half-adder and Diff. of half-subtracter.

The second applicable combination circuit is logic diagram of all-optical logic 2-to-4 lines decoder, shown in Fig. 3 (b). Likewise, output logic bit pattern is presented in Fig. 6 (a) and (b) as inputs of all-optical design, where Fig. 6 (c) output of NOR gate as D0, Fig. 6 (d) Boolean logic operation $\overline{A} \cdot B$ as D1, Fig. 6 (e) Boolean logic operation $A.\overline{B}$ as D2, and Fig.6 (f) output of AND gate as D3 of decoder outputs.

A successful logic operation for the targeted optical combination logic circuit is observed in Fig.5 and Fig.6. For a good performance of all-optical combinations logic design of each circuit, we are using PCs to control outputs of each combination circuit at the same time, where, λ_A, λ_B, λ_C, and a new generated wavelength are used for three optical logic combination circuits' outputs.

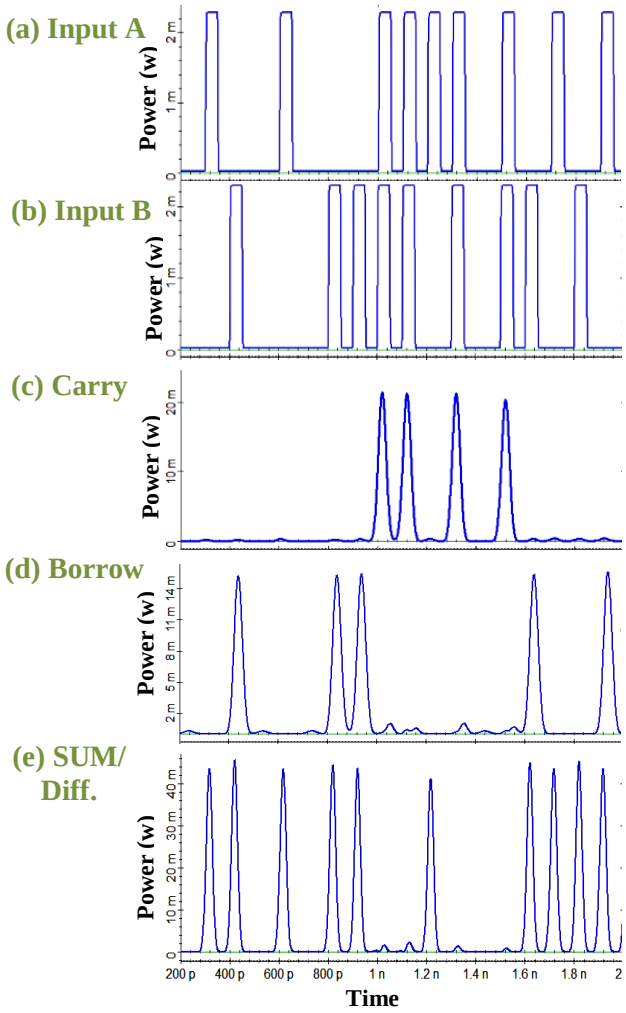

Fig. 5. Output logic bit pattern for all-optical logic 2-input half-adder/half-subtracter

Half-adder/half-subtracter are realized by a group of optical logic gates by adjusting filtering wavelengths of WDM outputs at 1550.918 nm (new generated wavelength obtained from FWM nonlinear effects), for AND gate to achieve CARRY operation with output power 22 mW, at 1550.116 nm for XOR gate to achieve SUM and Diff. operations as mentioned in Table 1, with output power of 46 mW. However, Borrow operation has two different logic operations dependent on arithmetic operations, where at 1551.72 nm, $\overline{A} \cdot B$ logic operation achieved for (B-A) and at 1552.524 nm, $A \cdot \overline{B}$ logic operation achieved for (A-B) with output power of 15 mW.

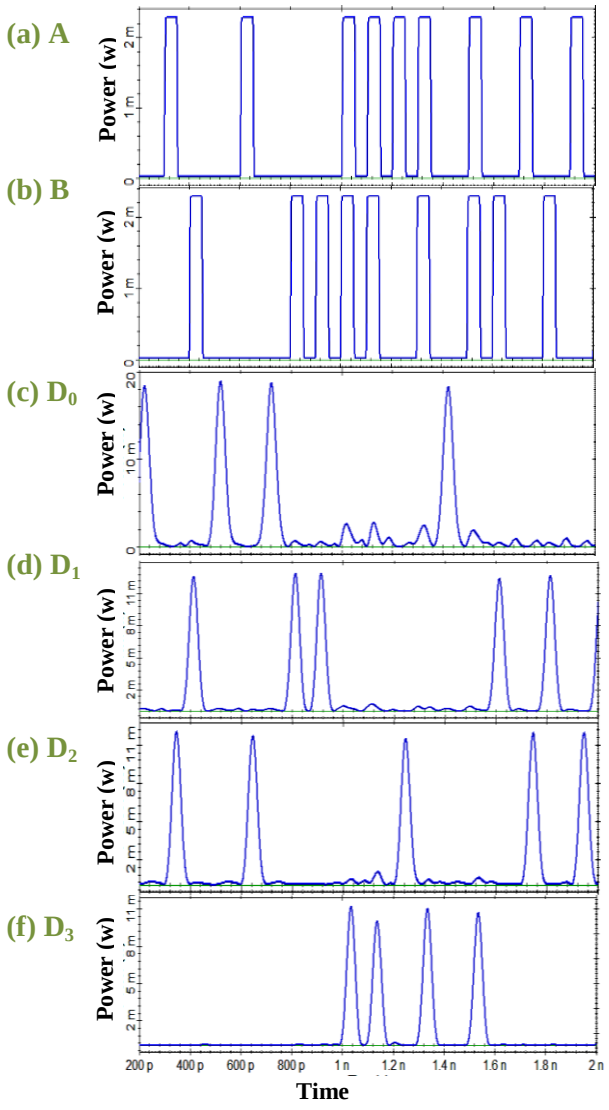

Fig. 6. Output logic bit pattern for all-optical logic 2-to-4 decoder

Nevertheless, four optical logic gates realize a 2-to-4 line decoder; three of them are demonstrated for half-adder/half-subtracter after controlling PCs with same criteria of orthogonal inputs. While outputs of D_1, D_2, and D_3 are achieved, as shown in Fig. 6, output of D_0 is realized by a NOR gate at 1550.116 nm, with average

output power levels for four output (D_0, D_1, D_2, and D_3) around 14 mW.

Error-Free operating system requires a manual entry of a-bit stream, which is achieved for 2^{31}-1 word length at 10 Gbps, utilizing novelty optimized low inputs power of 0.01 mW (-20 dBm) that realize a low harmonics level as shown in Fig. 7. This system consists of a PIN photodiode, an electric low pass filter (LPF), and a sampling /decision circuit [2, 23].

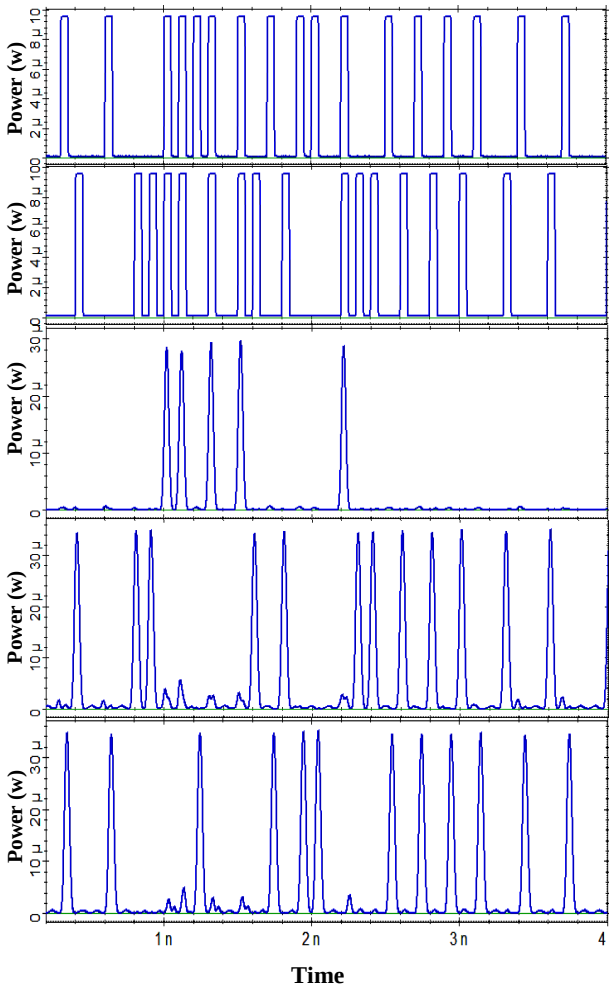

Fig. 7. Output logic bit pattern for all-optical common gates (AND,$A \cdot \bar{B}$, $\bar{A} \cdot B$) for 2^{31}-1 word length

A prominent BER of 10^{-12} is shown in Fig. 8, for example $\bar{A} \cdot B$, with a large eye that indicates a clear transmission, where the relative eye-opening (O) is defined as:

$$O = \frac{P^1_{min} - P^0_{max}}{P^1_{min}}$$

where "P^1_{min}" and "P^0_{max}" are the minimum and maximum powers at *1-state* and *0-state*, respectively [29, 30]. In addition, one of most important parameter is Q-factor, where the BER improves as (Q) increases and becomes lower than 10^{-12} for Q-factor above 7, as shown in Fig. 8.

The extinction ratio (ER) is extra information that is related to the BER and can be extracted from the eye-diagram. It is defined as the ratio of the power used to transmit a logic level '1' divided by the power used to transmit a logic level '0' [8]. The value of ER for all-optical combinational logic design is less than 25 dB, as shown in Fig.9. These values indicate a quit a good response of the circuit under consideration at its output terminals.

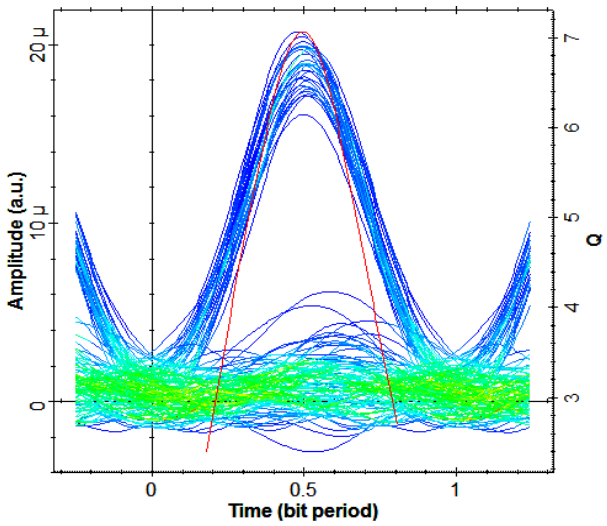

Fig. 8. Eye-diagram for all-optical operation $\bar{A} \cdot B$ with Q-factor 7.06 and eye opening factor 85.84%

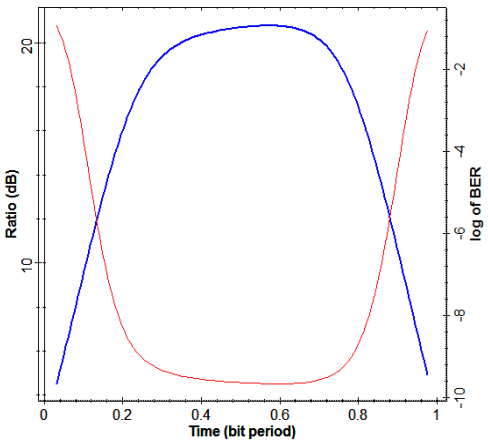

Fig. 9. Effects of optimized low inputs power on ER at 10^{-11} BER for AND gates

5. Comparison

This section presents the related work, including the design and simulation of several types of optical logic gates. Table 2 provides this review and can be used to establish a useful comparison between our work and the related studies.

The combinational circuit, bit rate, data formatting, and word length provide useful information about operating capacity/speed. A review of the power performance for the logic gates can be extracted from nonlinear (NL) techniques, and data power/probe power BER, ER and power penalty (Pp) are the evaluation parameters.

Table 2. Comparison between this work and related literature

	Operating Capacity			***Power Performance***		***Error-free***		**With SOA**	**Without SOA**	**Integration Capacity**
	Comb. Circuit	Bit rate (Gb/s)	Word Length	NL Technique	Data/ Probe Power	BER	ER/Pp (dB)			
[1] 2009	H.A/H.S	10	2^7-1	FWM	12-25 dB	10^{-9}	Pp =1.2	×	PPLN	Compact
[16] 2004	H.A	10	2^7-1	NA	27 dB	NA	ER =8	✓	×	Compact
[17] 2006	H.A	40/ RZ	NA	FWM	15/13 m W	NA	NA	✓	×	Moderate
[18] 2006	H.A	40/ RZ	NA	XPM/ XGM	11/-2.8 dB	10^{-9}	Pp >2	✓	PPLN	Compact
[19] 2011	H.A/H.S	10	2^{15}-1	FWM/ XGM	24.3 dB	NA	NA	×	HNLF	Moderate
[20] 2007	H.A/H.S	40/ RZ	2^7-1	XGM	100 m W	NA	Pp =2.1	✓	PPLN	Compact
[31] 2007	Decoder	40/ RZ	2^{31}-1	FWM/ XGM	2.6/0.6 mW	NA	ER =13	✓	×	Compact
This Work	**H.A/ H.S and Decoder**	**10/ RZ**	**2^{31}-1**	**FWM**	**0.01 m W**	**10^{-12}**	**ER=25**	**×**	**DCF**	**Moderate**

The complexity of different schemes in the literature is abbreviated in an integration capacity, where different design structures are compared according to nonlinear elements used, such as length of the fiber, circulators, filters, tunable filters, and SOAs.

In addition, some optical combinational circuits designed with HNLF/DSF, MZ interferometer, PPLN, and delay interferometer configurations, are larger than related designs, which make them inconvenient compared to digital circuits. Therefore, some gates using circulators, optical channel dropping filters, and tunable filters have reported fewer logical gates but are still compact in size.

From Table 2, although, we used 2^{31}–1 long word length for two different data signals, with low data/probe power requirement and commercial optical fiber link to demonstrate three different all-optical combinational circuits with four different logic gates, it is clear that the present work achieves better BER performance with eye opening factor 85.84% and moderate integration capacity.

6. Conclusion

We have built an all-optical combination logic design capable working with 10 Gbps RZ modulation data streams based on the FWM effect of single HNL-DCF. The proper behavior of the gates, as well as the quality of the output signals have been evaluated, derived and demonstrated. This allows a good aperture of eye diagrams for word length (2^{31}-1) after the optimized low data power requirement at 10^{-12} BER and ER above 25 dB.

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