

A Novel Power Converter with Voltage-Boosting Capacitors for a Four-Phase SRM Drive

Yasser G. Dessouky, Barry W. Williams, and John Edward Fletcher

Abstract— This paper presents a method of enhancing the performance of a four-phase switched reluctance motor by using capacitors to produce additional supply voltage during the rise and fall periods of a motor phase current. The voltage rating of the inverter components increases and extra capacitor/diode combinations are needed. The operation and analysis of a series voltage boost circuit are detailed for different modes of operation with a study of the effect of the boost capacitor voltage on the current waveform. Different voltage boost circuit configurations are compared. The predicted and measured results show that the boost circuit increases both torque and output power and, improves the efficiency of the machine, especially at high speeds.

Index Terms— Drives, power converter, switched reluctance motor, voltage boosting.

NOMENCLATURE

C	Boost capacitor, F.
D	Inductance rate of change, $H \cdot s^{-1}$.
i	Instantaneous phase current, A.
I_m	Flat-top level of the phase current, A.
L	Phase inductance, H.
L_u	Phase inductance at the unaligned position, H.
L_a	Phase inductance at the aligned position, H.
N_r	Number of rotor poles.
R	Resistance per phase, Ω .
V	DC supply voltage, V.
v_c	Instantaneous voltage across the boosting capacitor, V.
V_{co}	Initial voltage across the capacitor, V.
θ	Rotor position with reference to the unaligned position, rad.
θ_r	Rise angle of the current, rad.
θ_f	Fall angle of the current, rad.
θ_d	Discharging angle of the capacitor, rad.
ψ	Phase flux linkage, $V \cdot s$.
ω	Rotor angular velocity, $rad \cdot s^{-1}$.

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I. INTRODUCTION

SWITCHED reluctance motor (SRM) drives have been researched in the areas of motor principles, operation, and control [1]–[3]. Because of their cost advantages and ruggedness, these drives are suitable for high-speed applications. In this paper, a new power converter is presented that improves the high-speed performance of a four-phase SRM, by connecting capacitor/diode parallel combinations in series with the dc link. The capacitor stores the energy recovered from the phase winding during the current fall and pumps the stored energy back into the motor during current rise. This stored energy provides a boost voltage which squares up the current waveform, hence, increases the output power of the motor. This is particularly true at high speeds. Use of the voltage boost circuit has enhanced the performance of single-phase [4], [5] and two-phase [6] SRM's. Separate boost circuits have been employed in three or more phases [7]. For SRM's with three or more phases, it is not possible to use a single boost circuit, since overlapping phase currents prevent boost voltage buildup.

In this paper, the boost circuit in Fig. 1 uses two capacitors and two diodes with a four-phase SRM. Details of the SRM are given in Table I. The six-switch power converter [8] consists of two bridges where quadrature phases share a single-ended bridge leg. With such an arrangement, only one phase current flows through any switch at any time. The converter is suitable for boost circuit adaption because the currents in phases 1 and 3 are 180° electrically separated, as are the currents in phases 2 and 4. Therefore, each boost capacitor experiences a periodic current comprised of the two separate, individual currents. A model of the motor with and without the boost circuit, as derived from its differential equations, is presented. The three operating modes of the boost circuit are explained with a study considering the effect of the boost capacitor voltage on the current waveform. Experimental results are presented and performance curves are given. Boost circuits using two capacitor/diode combinations in parallel and using only one capacitor/diode combination in series are also considered.

II. SIMULATION OF THE SR DRIVE

A. Inductance Modeling

In an SRM, the inductance per phase changes from a minimum value L_u at the unaligned position to a maximum value L_a at alignment. The unaligned inductance is constant (current independent) since the magnetic circuit is dominated

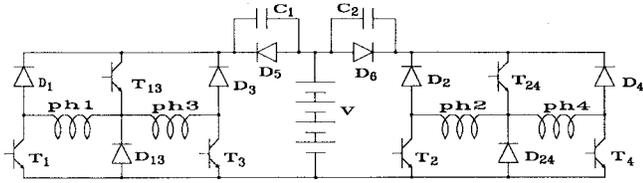


Fig. 1. The voltage boost circuit for a four-phase SRM drive using two diode/capacitor combinations in series.

TABLE I
ELECTRICAL PARAMETERS OF FOUR-PHASE SRM

No. of turns per phase = 710	Flat-top current, $I_m = 2.4$ A
Supply Voltage = 300 V	Phase resistance, $R = 9.6$
Unaligned inductance, $L_u = 79.6$ mH	Unsaturated aligned inductance = 216.2 mH

by large interpole airgaps. The aligned inductance is a function of current because of saturation effects in the iron parts. Using curve-fitting techniques on the flux linkage versus current data, the aligned inductance L_a as a function of the instantaneous phase current can be modeled as

$$L_a(i) = \begin{cases} 216.17 & i < 2.25 \\ 225.08 - 3.96i & i \geq 2.25 \end{cases} \text{ mH.} \quad (1)$$

If the inductance change from the unaligned to the aligned position is approximated by a cosinusoidal waveform, the instantaneous inductance as a function of the rotor position is given by

$$L(\theta, i) = \left(\frac{L_a(i) + L_u}{2} \right) (1 - \cos(N_r \theta)) \quad (2)$$

where the rotor position is related to time by

$$\theta = \omega t. \quad (3)$$

The inductance rate of change is given by

$$\frac{dL}{dt} = D(t, i) = \left(\frac{L_a(i) + L_u}{2} \right) N_r \omega \sin(N_r \omega t). \quad (4)$$

During simulations, the inductance L and its rate of change D [(1)–(4)], are updated for each instantaneous value of current and time.

The instantaneous torque per phase T_t is given by

$$T_t = \frac{1}{2} i^2 \frac{D}{\omega} \quad (5)$$

where the phase produces positive torque when the inductance rate of change is positive. The ideal current during this period, for maximum torque, given a maximum current limit, is rectangular, but this is not possible practically. In practice, both current rise and fall rates are limited by phase inductance and finite forcing voltages. Therefore, to obtain optimal torque from the motor, the phase current should rise from zero at the unaligned position to reach its flat-top level I_m in the minimal rise angle θ_r . Then, it is kept constant at this level until the fall angle θ_f , when the current starts to fall, reaching zero at the aligned position. The rise and fall angles are dependent on machine parameters, as well as the operating conditions.

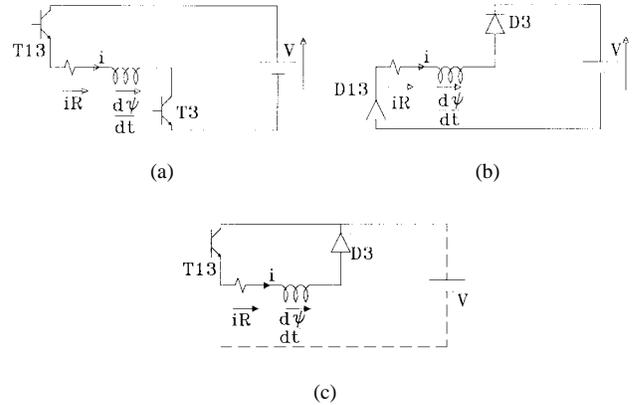


Fig. 2. Phase winding in (a) positive, (b) negative, and (c) zero voltage loops.

B. Current Prediction Without a Voltage Boost Circuit

The current rises when the phase experiences a positive voltage via switches T_1 and T_{13} [Fig. 2(a)]. The Kirchhoff's EMF equation is

$$V = iR + \frac{d\Psi}{dt} \quad (6)$$

and flux linkage is related to current by

$$\Psi = Li. \quad (7)$$

Substituting (7) into (6), and rearranging gives

$$\frac{di}{dt} = \frac{V - i(R + D(t, i))}{L(t, i)}. \quad (8)$$

The current falls when the phase experiences a negative voltage via diodes D_1 and D_{13} [Fig. 2(b)] and the EMF equation becomes

$$-V = iR + \frac{d\Psi}{dt}. \quad (9)$$

Substituting (7) into (9) and rearranging gives

$$\frac{di}{dt} = \frac{-V - i(R + D(t, i))}{L(t, i)}. \quad (10)$$

For low speeds, the back EMF $d\Psi/dt$ is small and, therefore, the current can be maintained at the flat-top level I_m by alternatively chopping the current in positive voltage loops [Fig. 2(a)] and zero voltage loops [Fig. 2(c)]. The higher the speed, the higher the back EMF and, consequently, the rise angle θ_r increases and the fall angle θ_f decreases, converging to the crossover speed ω_1 when $\theta_r = \theta_f$. For speeds higher than ω_1 , the current does not reach I_m , but attains a smaller value I_e . To find the current waveform for different speeds, the rise and fall angles are determined by solving the nonlinear differential equations (8) and (10), respectively. The necessary boundary conditions are given in Table II.

TABLE II
 BOUNDARY CONDITIONS FOR (8) AND (10)

	$\omega t =$	$i =$	$i =$
Eqn (8)	0	0	0
	θ_r	I_m	I_e
Eqn (10)	θ_f	I_m	I_e
	$\pi/6$	0	0
	-	-	$I_e < I_m$
	-	-	$\theta_r = \theta_f$

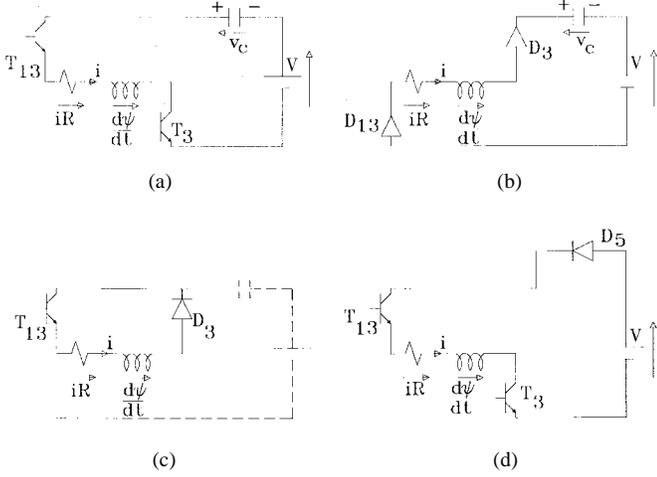


Fig. 3. Voltage boost circuit in (a) positive via capacitor, (b) negative, (c) zero, and (d) positive via diode voltage loops.

C. Current Prediction with a Voltage Boost Circuit

The current rises when the phase experiences positive voltage loops [Fig. 3(a)] while the boost capacitor is discharging. The EMF equation is given by

$$V + v_c = iR + \frac{d\Psi}{dt}. \quad (11)$$

Substituting (7) into (11) and rearranging yields

$$\frac{di}{dt} = \frac{V + v_c - i(R + D(t, i))}{L(t, i)}. \quad (12)$$

The boost capacitor voltage is related to the current by

$$\frac{dv_c}{dt} = -\frac{i}{C}. \quad (13)$$

The current falls in negative voltage loops [Fig. 3(b)], thereby charging the boost capacitor. The EMF equation is given by

$$V + v_c = -iR - \frac{d\Psi}{dt}. \quad (14)$$

Substituting (7) into (14) and rearranging

$$\frac{di}{dt} = -\frac{V + v_c + i(R + D(t, i))}{L(t, i)}. \quad (15)$$

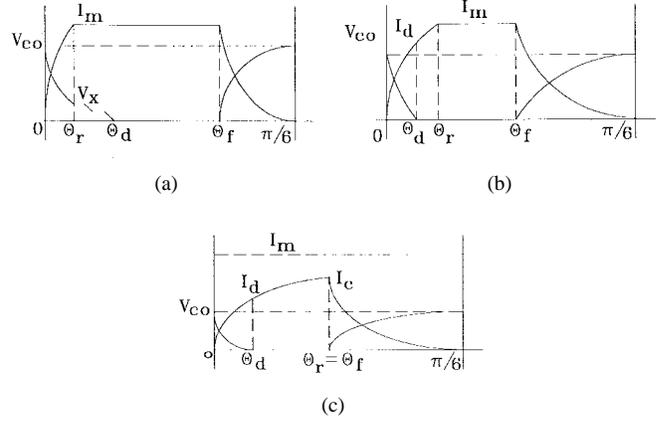


Fig. 4. Phase current and capacitor voltage waveforms for different modes of operation.

The boost capacitor voltage is related to the current by

$$\frac{dv_c}{dt} = \frac{i}{C}. \quad (16)$$

To obtain the current waveform, (12), (13), (15), and (16) are solved. The necessary boundary conditions are speed dependent, as will be shown in Section III. It is assumed that, during phase current rise periods, switching is dominated by positive voltage loops, while during current fall periods, the switching duty cycle is dominated by negative voltage loop operation.

Having determined the current waveform either with or without the voltage boost circuit, the torque, input power, output power, and the efficiency can be calculated [9], [10].

III. OPERATION MODES WITH THE VOLTAGE BOOST CIRCUIT

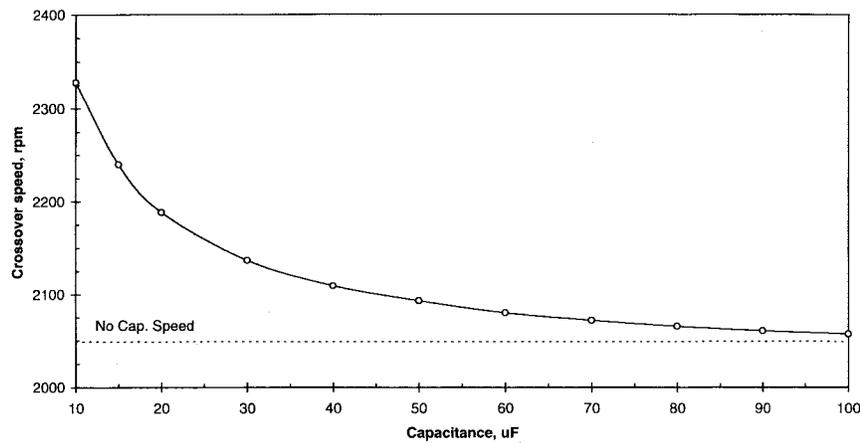
The voltage boost circuit has three modes of operation. Fig. 4 shows phase current and the capacitor voltage waveforms for these modes which are explained as follows.

A. Operation in Mode (1)

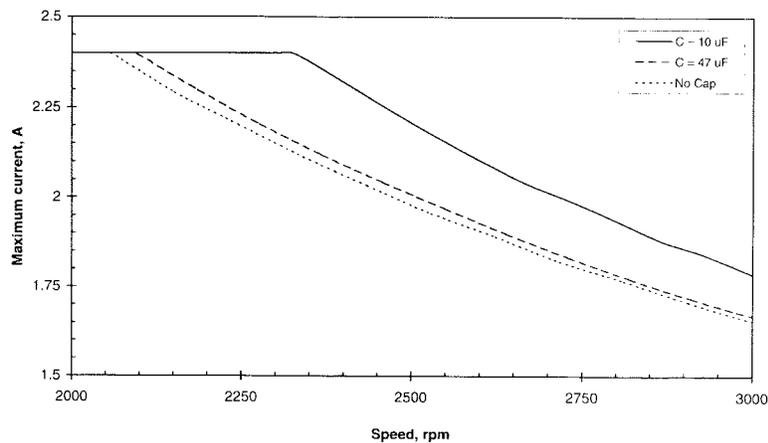
As shown in Fig. 4(a), with an initial voltage V_{co} across the boost capacitor at the unaligned position, the phase current starts to rise in positive voltage loops [Fig. 3(a)]. The current reaches I_m at the rise angle θ_r , while the capacitor does not discharge completely. The current is alternately chopped in zero voltage loops [Fig. 3(c)] and positive voltage loops [Fig. 3(a)]. Thus, in every positive voltage loop, the capacitor is discharging, while in the zero voltage loop, the capacitor voltage remains unchanged. This process is repeated until the capacitor voltage reaches zero at the discharged angle θ_d . Then, the boost circuit diode prevents the boost capacitor from charging negatively and it facilitates the positive loop current [Fig. 3(d)]. The current is chopped to maintain a flat-top level I_m until the fall angle θ_f . The current then falls in negative voltage loops [Fig. 3(b)] charging the capacitor. The phase current reaches zero at the aligned position, the capacitor voltage having reached V_{co} , which is the initial voltage for the next current cycle. At low speeds, a sufficiently long flat-top

TABLE III
BOUNDARY CONDITIONS FOR SOLUTION OF (12), (13), (15), AND (16)

	$\omega t =$	$i =$	$v_c =$	$\omega t =$	$i =$	$v_c =$	$\omega t =$	$i =$	$v_c =$
Eqn(12),	0	0	V_{co}	0	0	V_{co}	0	0	V_{co}
(13)	θ_r	I_m	$V_x > 0$	θ_d	I_d	0	θ_d	I_d	0
Eqn (8)	-	-	-	θ_d	I_d	-	θ_d	I_d	-
	-	-	-	θ_r	I_m	-	θ_r	I_e	-
Eqn(15),	θ_f	I_m	0	θ_f	I_m	0	θ_f	I_e	0
(16)	$\pi/6$	0	V_{co}	$\pi/6$	0	V_{co}	$\pi/6$	0	V_{co}
	-	-	-	-	-	-	$\theta_r = \theta_f$	$I_e < I_m$	-



(a)



(b)

Fig. 5. The relationship between (a) crossover speed and boost capacitance and (b) maximum phase current.

current period exists to fully discharge the boost capacitor. This mode continues as the speed increases, until $\theta_d = \theta_r$, such that the current I_m is reached just as the boost capacitor voltage reaches zero.

B. Operation in Mode (2)

In this second mode [Fig. 4(b)], the current starts to rise in the positive voltage loops of Fig. 3(a), discharging the capacitor from V_{co} at the unaligned position to zero at a current

level I_d , which is lower than I_m . The current continues to rise until θ_r , but the positive loop current is supplied via the diode D_5 from the supply V , as implied by (8). The current is chopped in alternating zero and positive loops as in Fig. 3(c) and (d), respectively, until θ_f . The current fall period (i.e., $\theta_f \leq \theta \leq \pi/6$) resembles that of mode (1). Increasing motor speed increases the rise angle and decreases the fall angle until the crossover speed ω_1 when the rise angle θ_r is coincident with the fall angle θ_f .

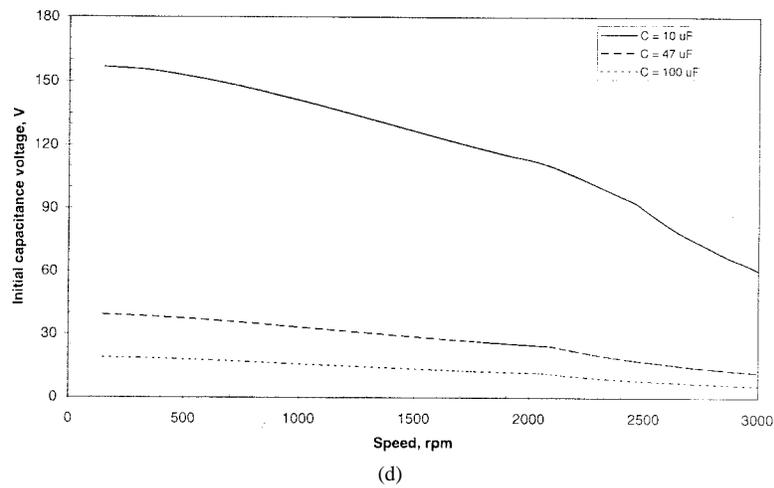
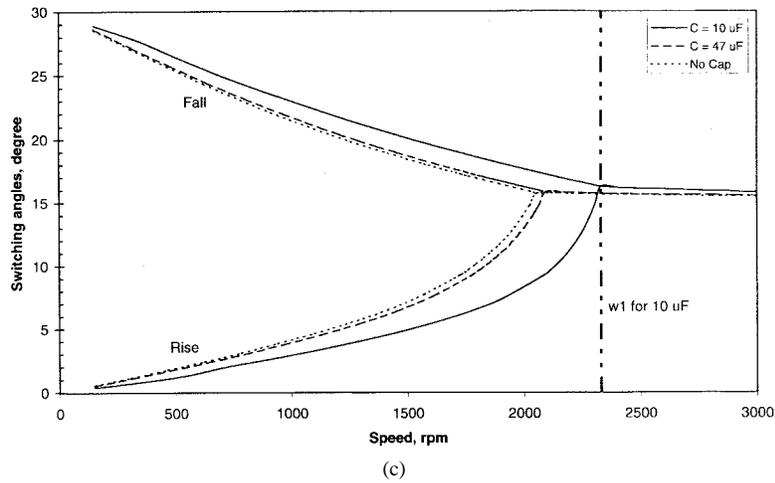


Fig. 5. (Continued.) The relationship between (c) switching angles and (d) capacitor initial voltage versus speed for different boost capacitance.

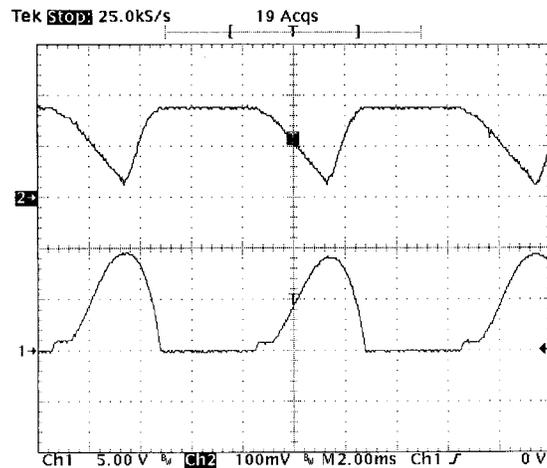


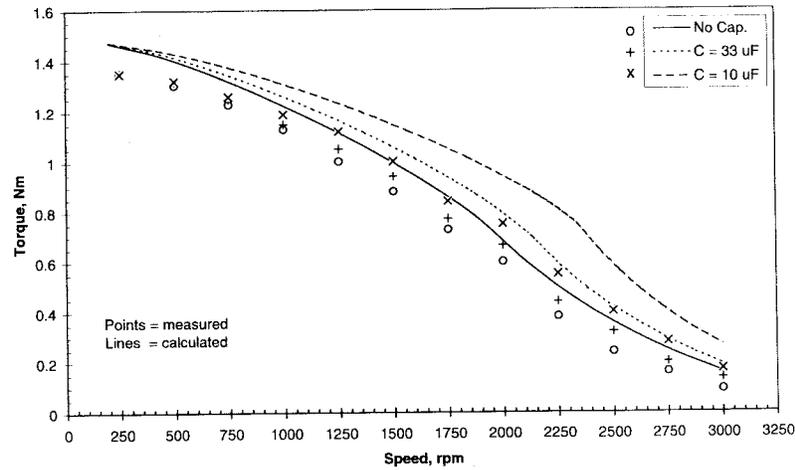
Fig. 6. Experimental phase current and capacitor voltage waveforms: 2 ms/div, upper trace 1 A/div, and lower trace 50 V/div.

C. Operation in Mode (3)

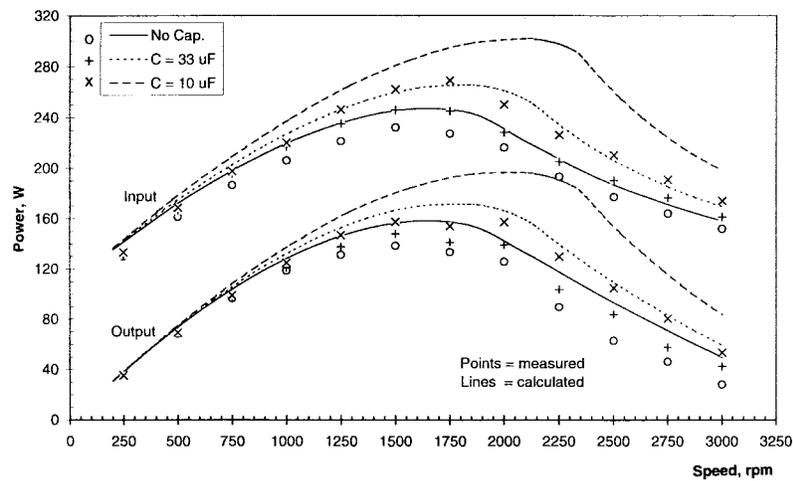
For speeds higher than ω_1 , the back EMF is high and, therefore, the current has insufficient time to reach I_m , but rather attains a smaller value I_e , as shown in Fig. 4(c). This

third mode, in analysis, resembles *Mode (2)*, except that no flat-topped chopping period exists.

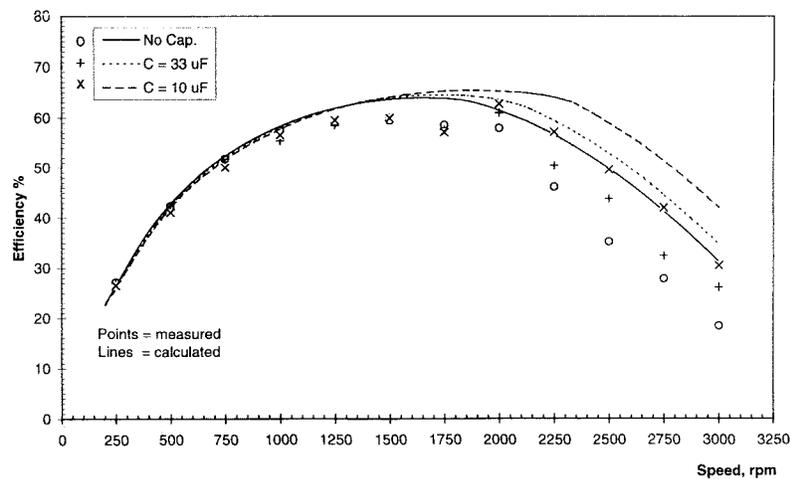
The initial conditions of the differential equations which determine the current waveform for each mode are given in Table III.



(a)



(b)



(c)

Fig. 7. Torque, power, and efficiency versus speed for different boost capacitance.

IV. EFFECT OF BOOST CAPACITOR VOLTAGE ON THE CURRENT

The current waveform depends on the motor operating conditions. The major factor affecting the waveform is the boost capacitance magnitude. As explained in Section III, the

rise angle is coincident with the fall angle at the crossover speed ω_1 , after which the phase current does not reach I_m . Fig. 5(a) shows the relationship between crossover speed and boost capacitance. It is seen that the lower the capaci-

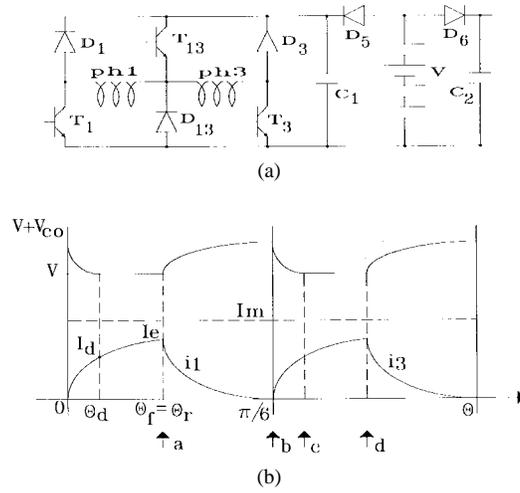
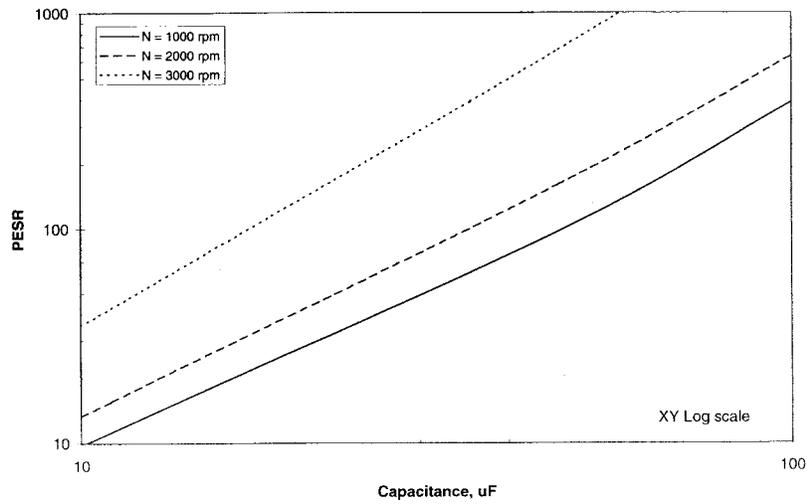
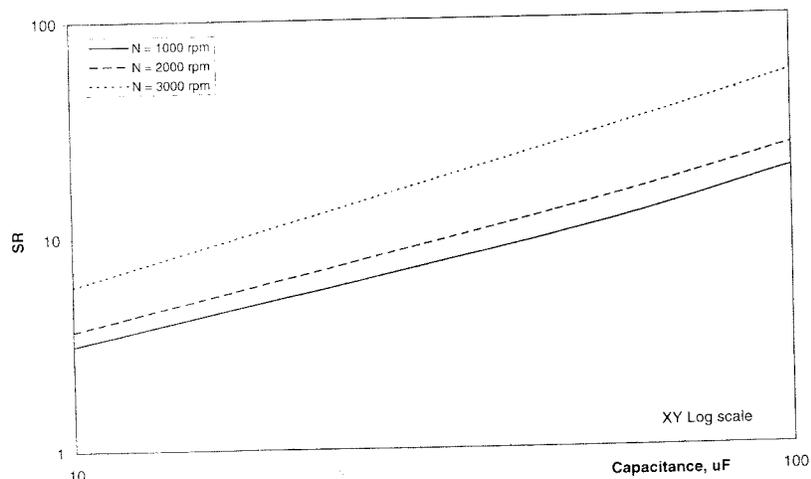


Fig. 8. (a) Circuit diagram and (b) phase current and capacitor voltage waveforms for the parallel capacitor voltage boost circuit.



(a)



(b)

Fig. 9. PESR and SR versus boost capacitance.

tance, the higher the crossover speed. The maximum phase current is I_m for speeds lower than ω_1 and I_e for speeds in excess of ω_1 . The relationship between maximum phase

current and speed, shown in Fig. 5(b), indicates that decreased capacitance increases the maximum phase current for high speeds. Decreased capacitance also decreases the rise angle

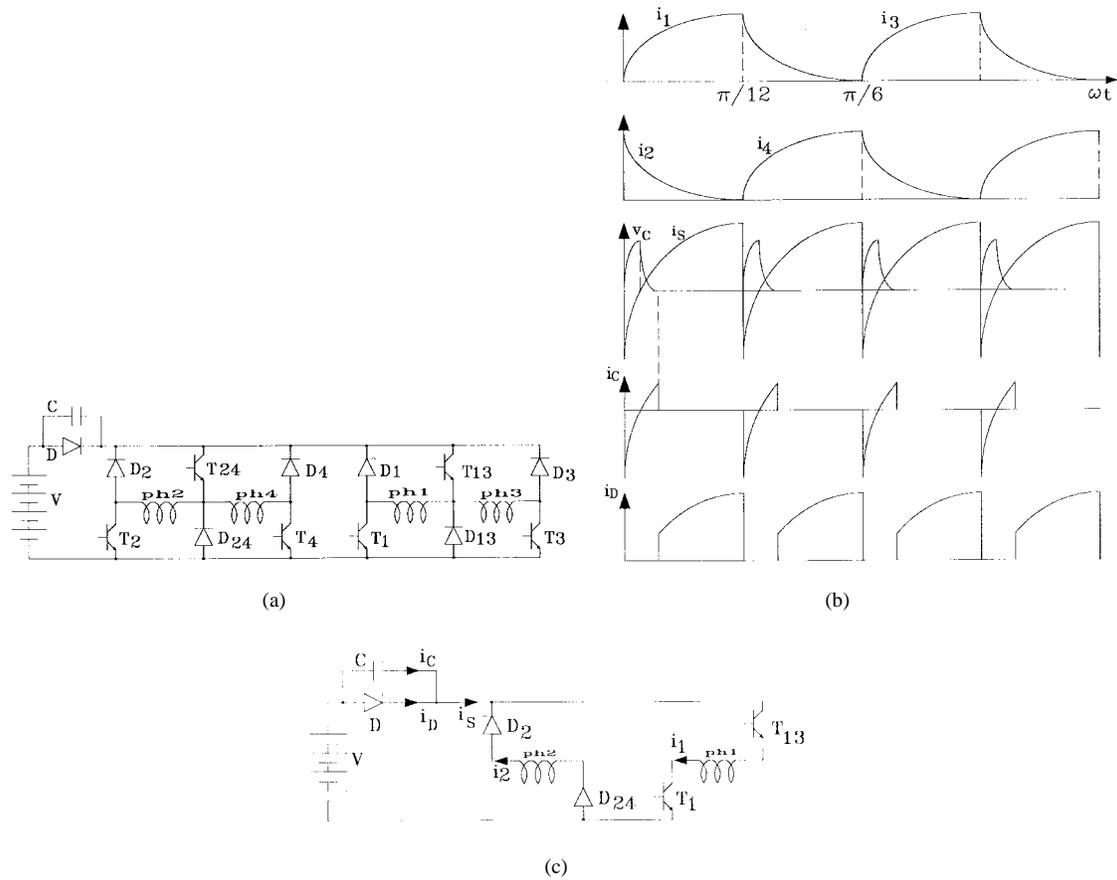


Fig. 10. (a) Circuit diagram, (b) current waveforms, and (c) energy exchange illustration for the one diode/capacitor voltage boost circuit.

and increases the fall angle for low speeds, as shown in Fig. 5(c). From the previous relationships, it is established that the boost capacitance increases the current waveform area and, hence, developed torque. The maximum voltage across the capacitor is the initial voltage V_{co} at the unaligned position. Thus, the maximum reverse voltage across any switch or bridge diode will be $(V + V_{co})$. Fig. 5(d) shows the relationship between V_{co} and speed. It illustrates that the lower the capacitance, the higher the initial capacitor voltage and, consequently, the higher the necessary voltage ratings of the inverter components.

V. PRACTICAL PERFORMANCE OF THE DRIVE

Fig. 6 shows typical experimental phase current and boost capacitor voltage waveforms. The performance of the machine on load with and without voltage boosting is recorded and compared with the simulation results. Motor speed dependence of developed torque, output and input power, and the efficiency are shown in Fig. 7. It is clear that voltage boosting increases the output power and enhances the efficiency of the machine, especially at high speeds where the maximum attainable phase current is increased. At a speed of 2000 r/min, a boost capacitance of 10 μF improves output power and efficiency by 25.2% and 8.2%, respectively. Differences between calculated and measured performance in Fig. 7 can be attributed to errors introduced due to the simple model used and the neglect of windage, friction, eddy currents, and hysteresis losses.

VI. PARALLEL BOOST CIRCUIT

Fig. 8(a) shows the four-phase drive circuit with two parallel boost circuits. It has been concluded [6] that the operation of the parallel boost circuit is similar to the series version for single- and two-phase SRM's. The phase current and capacitor voltage for one bridge of the four-phase SRM at high speed are shown in Fig. 8(b). The diode D_5 blocks current in *phase 1* when the current is falling via D_1 and D_{13} . Therefore, the energy in this phase is stored in the boost capacitor, such that the capacitor voltage rises from the supply voltage V at point *a* to $(V + V_{co})$ at point *b*. The current in *phase 3* now rises via T_3 and T_{13} , discharging the boost capacitor to V , where the diode D_5 comes into conduction at point *c*. Then, *phase 3* is fed directly from the dc supply between time points *c* and *d*. Comparing Fig. 8(b) with Fig. 4(c), it is seen that, for the same capacitance, the motor performance with the series and parallel boost circuits is similar, except that the maximum capacitor voltages for the series and parallel connections are V_{co} and $(V_{co} + V)$, respectively. The peak stored energy, hence, size for the parallel and series connected capacitors E_p and E_s , respectively, are given by

$$\left(\begin{array}{l} E_p = \frac{1}{2}C(V_{co} + V)^2 \\ E_s = \frac{1}{2}CV_{co}^2 \end{array} \right). \quad (17)$$

The peak stored energy ratio (PSER) for the same boost

voltage, hence, capacitance value, can be expressed as

$$\text{PSER} = \frac{E_p}{E_s} = \left(1 + \frac{V}{V_{co}}\right)^2. \quad (18)$$

The physical size ratio (SR) related to $C \times V$ (i.e., Q) is given by

$$\text{SR} = \frac{Q_p}{Q_s} = 1 + \frac{V}{V_{co}}. \quad (19)$$

The relationships between PSER, SR, and boost capacitance are shown in Fig. 9. This figure illustrates that, advantageously, the stored energy rating and the physical size of the series boost capacitor are always less than that of the parallel capacitor. One advantage of the parallel boost circuit is that the voltage supply need not be a reversible source. This is only important for one- and two-phase motors. In higher phase number motors, other conducting phases act as the returned energy sink.

VII. BOOST CIRCUIT USING ONE BOOST CAPACITOR

Fig. 10(a) and (b) shows a boost circuit for the four-phase SRM drive using only one capacitor/diode combination and the current waveforms, respectively. The experimental results confirm that the voltage boost circuit is ineffective. The reason can be attributed to the fact that energy exchange takes place between two conducting phases rather than one phase and the boost capacitor. As shown in Fig. 10(c), for high speeds where boosting is dominant, when the current in *phase 2* is falling, the current in *phase 1* is rising. Therefore, the recovered energy from *phase 2* is divided between *phase 1* and the capacitor/supply.

VIII. CONCLUSION

The performance of a four-phase SRM has been enhanced by means of two series capacitive voltage boost circuits. The circuit was modeled for three different operating modes. The study of boost capacitor effects on phase current indicates that decreasing the capacitance increasingly improves performance. However, higher voltage rated inverter components are required. At a speed of 2000 r/min, a 10- μ F capacitor increases motor output power and efficiency by 25.2% and 8.2%, respectively. Parallel boosting resembles series boosting in analysis, but the latter has the advantage of having a lower stored energy, hence, lower capacitor voltage rating, for the same value of capacitance. Using only one boost capacitor is not effective because energy exchange takes place between two adjacent conducting phases, rather than solely between the phase and the boost capacitor.

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