

DESIGN AND IMPLEMENTATION OF DATA ACQUISITION INTERFACING CIRCUIT FOR FIELD ORIENTED CONTROL SYSTEMS

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Abstract: This paper presents design and implementation of data acquisition interfacing circuits for signals of drive systems controlled via field orientation technique. System signals include speed and currents measurement and control signal to drive the power switches of the inverter. The circuitries include digital & analog devices to provide simple and fixable interfacing.

1. Introduction

To implement the field-oriented control of the induction motor, there is a major need for data acquisition interfacing to allow for the execution of the control algorithm & to output switching of the inverter. The implementation includes analog and digital hardware and software^{1,2}). In this paper, the hardware and software are designed and implemented for different measurements of speed and currents in addition to delivering the control signals to the driving circuit of the inverter. The interfacing circuits are intended to provide a flexible tool to field oriented control of induction motors to satisfy high flexibility.

During design it is noted to have a flexible instrumentation system to allow various high accuracy measurements of a number of variables in the drive system as shown in Fig.1 . The data acquisition interfacing circuits compose of AD/DA interfacing circuit and digital I/O circuit³). The conversion of the input and output signals to the drive system is executed by using a APC/2/6 ADDA card 16 channel input and 4 channel output in addition to a DM-P076 ADDA card of 16 channel input and 2 channel output for the purpose of tracing signals of the control program (Appendix A). To overcome multiplexer delay problem a delay loop is introduced between any two outputs. The ADDA cards have been used for the following :

- (1) Output three phase sine wave pulses result from PI controllers.
- (2) Read two phase current i_a and i_b .
- (3) Read speed command signal.

2. Digital Interfacing

A digital interfacing card has been designed and implemented for digital interfacing and timing^{2, 4}) This card is driven by the I/O bus of the microprocessor and is programmed by the microprocessor to determine which of the ports will exchange information with the I/O bus.

Figure 2 describes the digital interfacing circuitry which has been implemented using standard ICs. The digital card has been designed to interface the CPU to the digital signals of the system as in the following :

- (1)Monitoring the switches state.
- (2)Reading time duration.
- (3)Speed measurement and speed estimation.

On the digital interfacing card, the Intel 8255A programmable peripheral interface (PPI) chip is used as a typical I/O chip. This chip includes a programmable control register which in turn controls the configuration of the three 8-bit ports. The microprocessor can address and write to the control register over the bi-

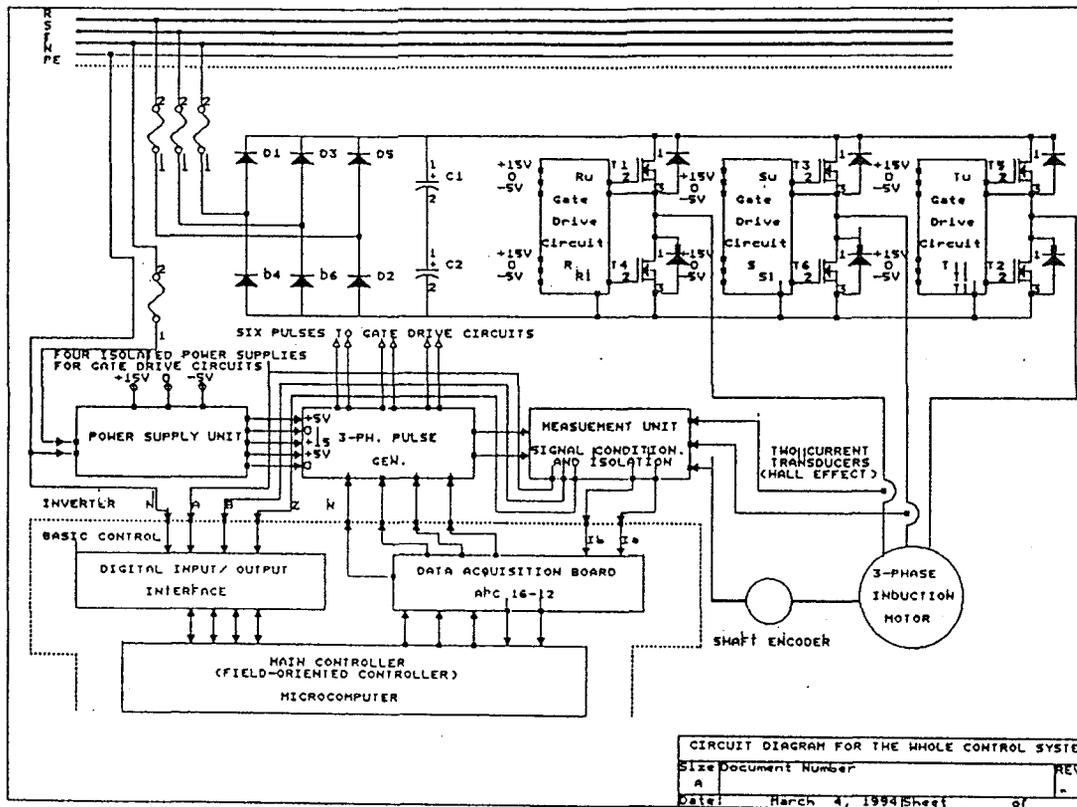


Fig. 1 Circuit diagram of the drive system

directional data bus to initialize the configuration of all lines of the three ports. As timing is important for the designed control system, the digital interface board also includes the Intel 8253 programmable interval timer (PIT). This PIT includes three independent 16-bit down counters that can count down at any frequency up to 3 MHz.

The above requirements are carried out employing the Programmable Peripheral Interface (8255), the programmable interval timer (8253), and other auxiliary chips for buffering and decoding. Each programmable chip has been programmed according to its function as follows:

1-Programmable peripheral interface (PPI)

Port A is assigned for monitoring switch signals. Ports B and C_{upper} are utilized to output the estimated frequency from the CPU to the seven segment display (digits). Port C_{lower} is employed to read output of the sampling timer signal.

2- Programmable interval timers (PIT)

Two PIT(8253) have been employed to estimate the time required for the control program. Implementing a timer T0 (PIT1) for the integration part of the flux estimation, while timer T1 (PIT1) for the integration part of PI controller. Timer T2 (PIT1) is used to produce a signal every sampling time to start execution of the program. Timer T0 (PIT2) is assigned for speed estimation (Sec.4).

The programmable digital interfacing chips require a decoding circuit to initialize and select any of PPI and PIT for operation. The chip that has been used for addressing is the address decoder 74LS138.

3. Speed Measurement

Speed detection is based upon the high precision speed detection method (M/T) which is designed and

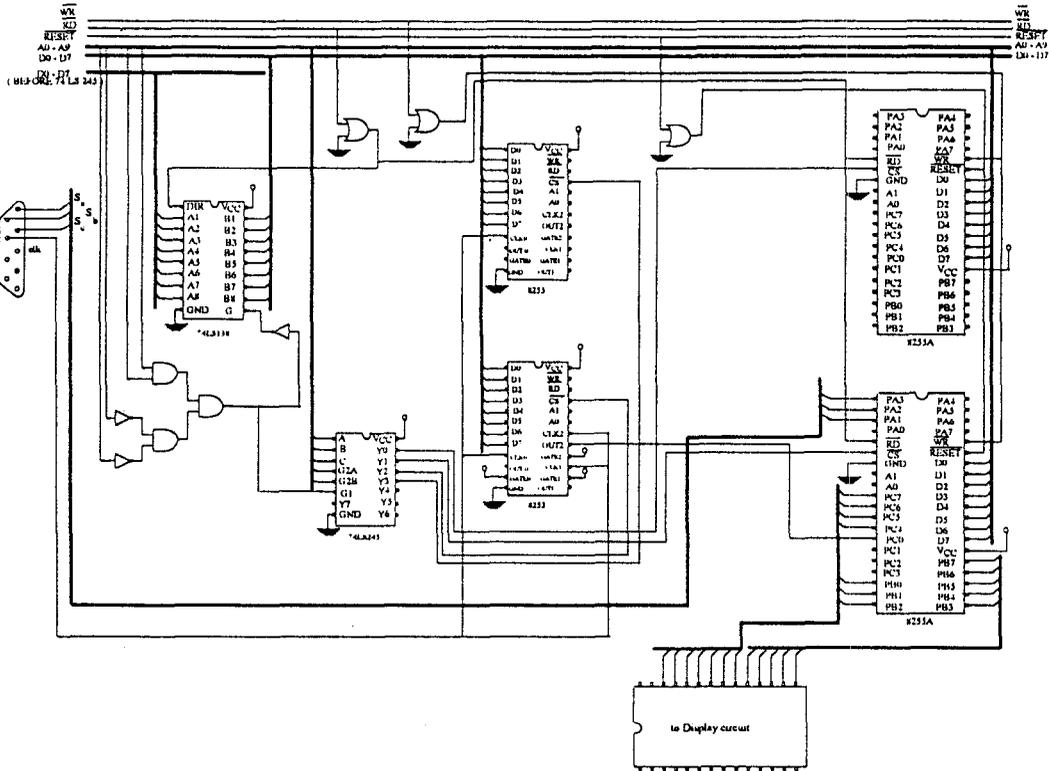


Fig. 2 Digital interfacing circuit

implemented to connect the shaft encoder to the microcomputer. Design and implementation ensure that the speed detecting system can meet the requirements of fast response and high accuracy. The main elements of speed measurement are shown in Fig.3 5). Counter#0 in the PIT is used to count the number of pulses m_1 coming from the frequency multiplier prepared for the encoder pulses. Counter#1 counts the pulses from the frequency reference circuit which uses a crystal oscillator of 2.097 MHz for less relative error in this design. The multiplier in the first stage is introduced to amplify the count of the pulses and so increase the resolution of measurement, consequently reduces the error. Counter#2 is used as a timer to obtain the interrupt signal of speed detection.

The process of counting is synchronized to the encoder pulses. The counting is finished at the occurring of the end of the speed sampling time which is adjusted by a timer. In addition this pulse becomes an interrupt signal for the microprocessor. After initializing the interrupt request, the microprocessor executes the detection process according to the flow chart shown in Fig. 4 to obtain the speed, position and $\sin(p)$ and $\cos(p)$ generation which are needed for field orientation controller 3).

4. Position and Speed Detection

If speed sensorless drive system is required, position and speed detection must be carried out 6). A novel simplified position and speed detection method depending on the comparator reference signal have been proposed. This technique leads to simplify the control system as hardware which results from absence of the speed sensor or any other sensor for speed detection. This approach simplifies the software algorithm which results from using a fast process to estimate the speed.

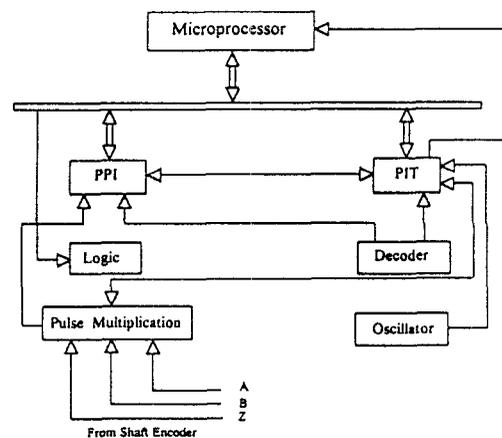


Fig. 3 Main blocks of speed detection circuit

The rotor speed can be computed by using estimation of the synchronous speed and slip speed. Synchronous speed has been estimated using the basics of the proposed novel technique while slip speed has been obtained by referring to field oriented equation.

Figure 4 illustrates the speed estimation routine as a function of measured sampling time (t). The speed is update 12 times each cycle, so updating time is a function of the inverter frequency. Therefore, this technique can be used in either low frequency and high frequency operation, the main advantage is its accurate estimation as the frequency increases which can't be exist in any other techniques that uses speed measurement or speed estimation.

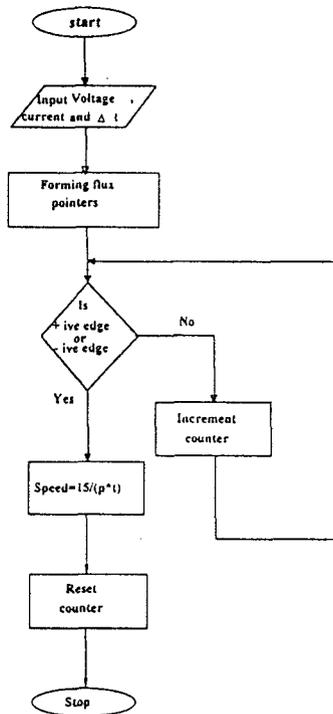


Fig. 4 Flow chart of speed estimation routine

5. Detection of Current Vector

The motor currents are measured in two phases and the current signal of the third phase is taken as the negative of the sum of these two currents because the motor has an isolated neutral point. The used current transducers employ the Hall effect phenomenon and provide a complete isolation between the power side and the control side. From the two measured currents i_{as} and i_{bs} the current space vector components $i_{qs}e^{*}$ and $i_{ds}e^{*}$ are calculated in the program as shown in the flowchart of Fig. 5.

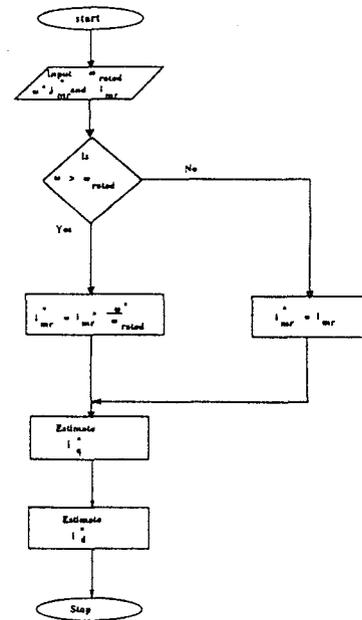


Fig. 5 Flow chart of current command i_q^* , i_d^* estimation

The measured signals are converted to digital form by the *APC 16-12 ADDA* board at the board input. Complete specifications of the *ADDA* board are presented in Appendix A. Figure 6 shows the hardware configuration for estimation of the current components, speed and position detection that are used to compute the current vector in the rotating reference frame.

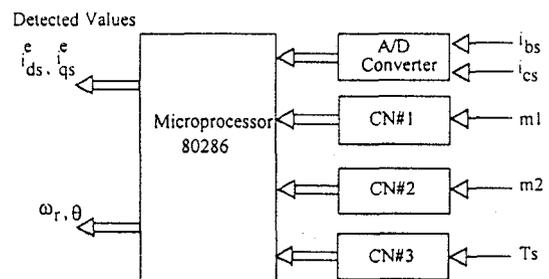


Fig. 6 Hardware Configuration of current detection

In the detection of the current component, the torque producing component of current i_{qs} , and the current representing the rotor flux, i_{ds} , are calculated from the detected values of the three-phase motor currents and angular rotation of the reference frame. Motor currents produced by the *PWM* inverter are not exactly sinusoidal; they have high-frequency components due to the switching of the *MOSFETs*. Therefore, the sampling was selected not to coincide with the switching of the transistors.

6. Control Signals

Three control signals are required to drive the power switches of the inverter. Such control signals are generated by intersection of three reference signals and a triangular wave as a carrier. The reference signals are produced by the control algorithm of F.O. controller in the microcomputer in such a way to keep them very close to sinusoidal form. Digital to analog converter (Appendix A) carries out the conversion of the reference signals to analog form which fed to be compared with the carrier wave for producing PWM pulses. The PWM pulses are inverted with delay time - via three phase pulse generator (Fig. 1)- to ensure avoidance of short circuit on the d.c. bus of the drive system.

7. Conclusion

Data acquisition interfacing circuitries have been designed & implemented to apply field orientation control technique on induction machine drive systems. The circuitries have satisfied all requirements of the drive systems and the applied control technique keeping high accuracy, flexibility and simplicity.

Appendix (A)

ADDA CARDS SPECIFICATIONS

ADDA APC-1612 SPECIFICATIONS

D/A Converter

Analog Output: 4 multiplexed channels
Voltage Range : 0-5 V, 0-10 V unipolar
+/- 2.5 V, +/- 5 V, +/- 10 V bipolar
Resolution : 12 bit
Linearity Error : $\pm 1/4$ LSB
Settling Time : 500 ns

A/D Converter

Analog Input 16 single-ended or 8 differential channels (equipped with sample-and-hold amplifier)
Voltage Range 0-5 V, 0-10 V unipolar
+/- 2.5 V, +/- 5 V, +/- 10 V bipolar
Resolution : 12 bit
Conversion Time : 25 μ s

ADDA DM-P076 SPECIFICATIONS

D/A Converter

Analog Output : 1 channel
Voltage Range : 0-5 V, 0-10 V unipolar
Resolution : 12 bit
Settling Time : 30 μ s

A/D Converter

Analog Input : 8 Single-Ended
Voltage Range : -5 V to +5 V bipolar

Resolution : 12 bit
Accuracy : 0.01% of reading ± 1 bit
Conversion Time : 25 μ s
Digital Inputs
6 Channels
Digital Outputs
16 Channels

8. References

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