ACADEMY FOR SCIENCE & TECHNOLOGY
COLLEGE OF ENGINEERING & TECHNOLOGY
Department : Computer Engineering Department
Course : Computer Architecture
Course Code: CC 311
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Sheet #3

1. Describe the effect that a single stuck-at-0 fault would have for the signals shown below in the single-cycle datapath. Which instructions, if any, will not work correctly? Explain why.

   Consider each of the following faults separately:

   a. RegWrite = 0
   b. ALUOp0 = 0
   c. ALUOp1 = 0
   e. MemRead = 0
   d. Branch = 0
   f. MemWrite = 0

2. Specify the instruction that is performed given the following control lines

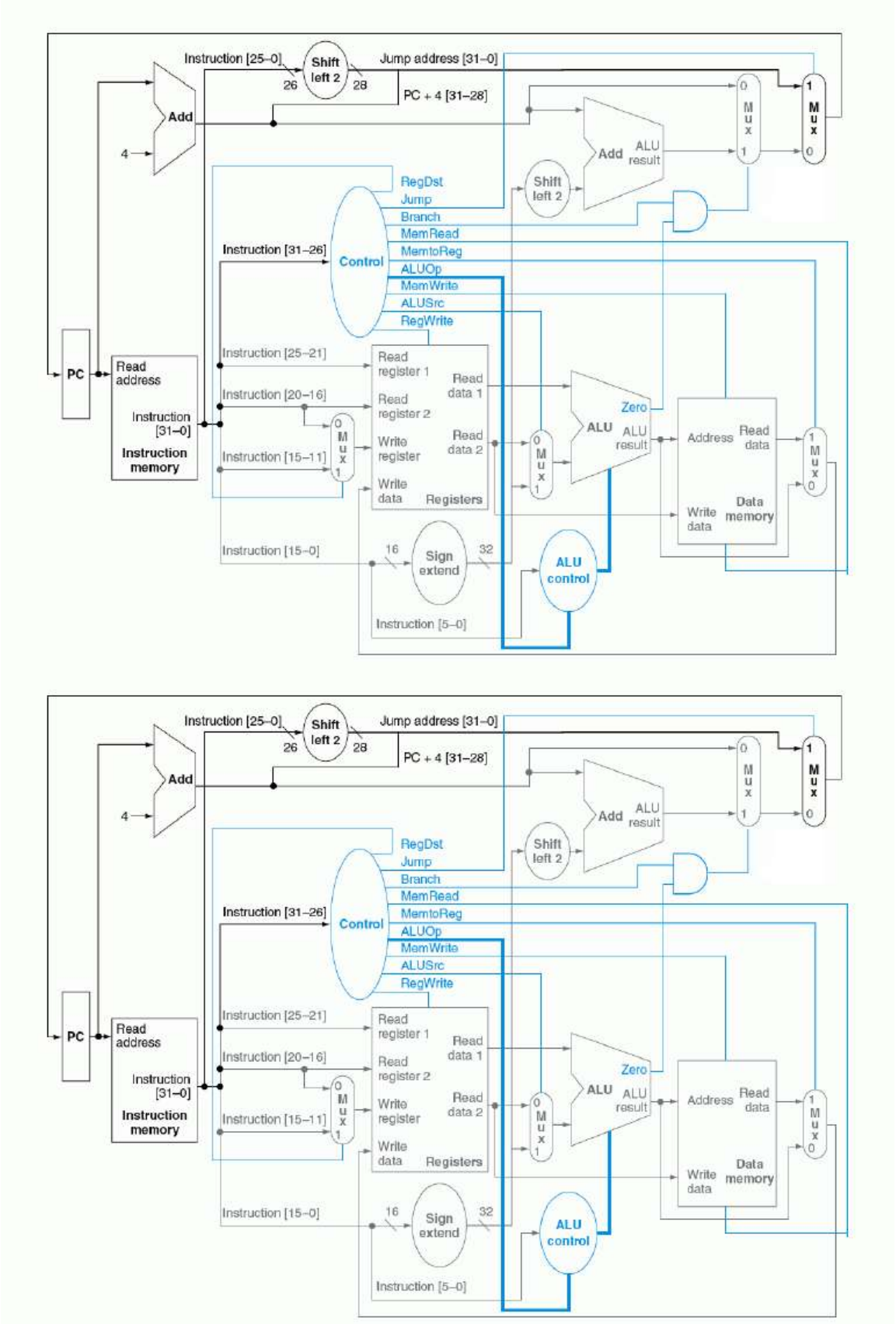
Regdst	Jump	Branch	MemRead	Memwrite	Memto Reg	Aluop	AluSrc	RegWrite
1	0	0	1	0	1	00	0	1

3. We wish to add the following instructions to the single-cycle datapath described. Add and show any necessary datapaths and control signals to the single-cycle datapath .
   a. Addi (add immediate)
   b. Bne (branch if not equal)

4. We wish to add a variant of the Lw (load word) instruction, which sums two registers to obtain the address of the data to be loaded and uses the R-format. Add and show any necessary datapaths and control signals to the single-cycle datapath .

5. Assume the new MIPS instruction **SWI** (store word immediate). Add and show any necessary datapaths and control signals to the single-cycle datapath . (Aluop for add operation=00)

Swi register(rs), register(rt), immediate
M [rs+rt]←immediate


Instruction [25–0]
Shift left 2
26
28
Jump address [31–0]
PC + 4 [31–28]
Add
4
M u x
0
1
Add
ALU result
Shift left 2
RegDst
Jump
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign extend
32
ALU
Zero
ALU result
ALU control
Address
Read data
Write data
Data memory