



ACADEMY FOR SCIENCE & TECHNOLOGY
COLLEGE OF ENGINEERING & TECHNOLOGY

Department : Computer Engineering Department

Course : Computer Architecture

Course Code: CC 311

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Sheet #4

1. Describe the effect that a single stuck-at-0 fault would have for the signals shown below in the multi-cycle datapath. Which instructions, if any, will not work correctly? Explain why.

Consider each of the following faults separately:

- | | |
|-----------------|-----------------|
| a. RegWrite = 0 | b. IRWrite = 0 |
| c. ALUSecA = 0 | d. MemRead = 0 |
| e. ALUSrcB = 0 | f. MemWrite = 0 |

2. We wish to add the following instructions to the multi-cycle datapath described. Add and show any necessary datapaths and control signals to the single-cycle datapath .
 - a. Addi (add immediate)
 - b. Bne (branch if not equal)
3. We wish to add a variant of the Sw (Store word) instruction, which sums two registers to obtain the address of the data to be stored and uses the R-format. Add and show any necessary datapaths and control signals to the multi-cycle datapath .
4. Assume the new MIPS instruction **SLTI** (set less than immediate). Add and show any necessary datapaths and control signals to the multi-cycle datapath.
(Aluop for add operation=00)
5. Assume the new MIPS instruction **ADDM** (add register to memory). Add and show any necessary datapaths and control signals to the multi-cycle datapath .
(Aluop for add operation=00)

addm **register(rs), register(rt), immediate**
rt ← **rs + M [immediate]**

